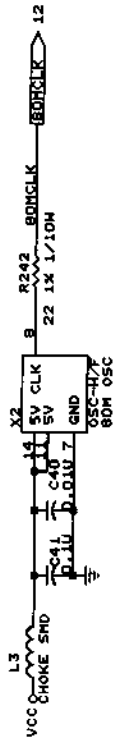


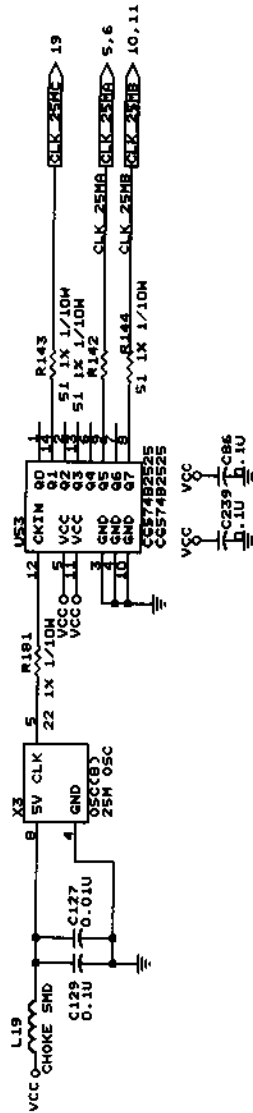
[illegible]

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		ED-1	



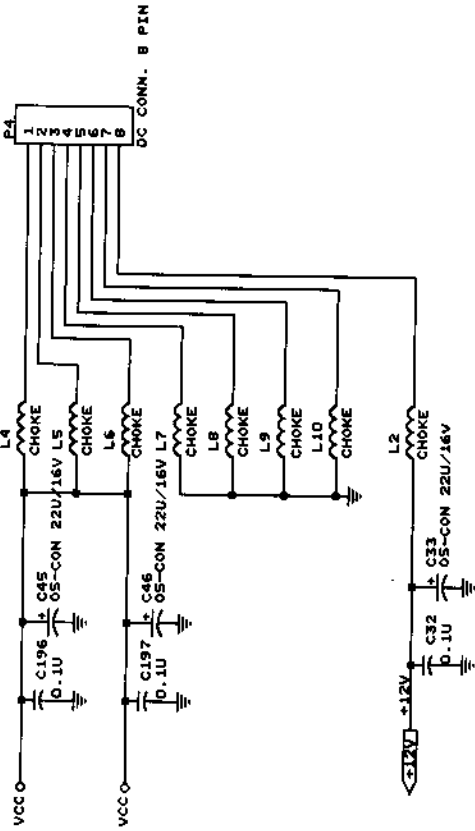
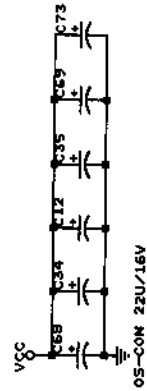


PLACED AS CLOSE AS POSSIBLE TO GT-48001A  
80 MHz FOR GT-48001A

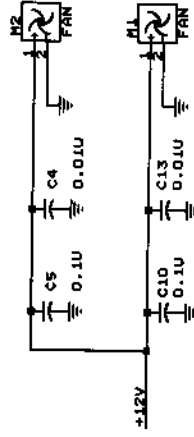


LAYOUT TRACES TO 4 LXT970  
SHOULD BE AS SHORT AS POSSIBLE

25MHz CLOCK FOR 4 LXT970

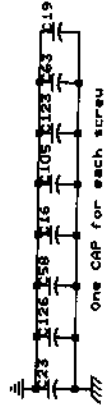


## POWER CONNECTOR



## FAN CONNECTORS

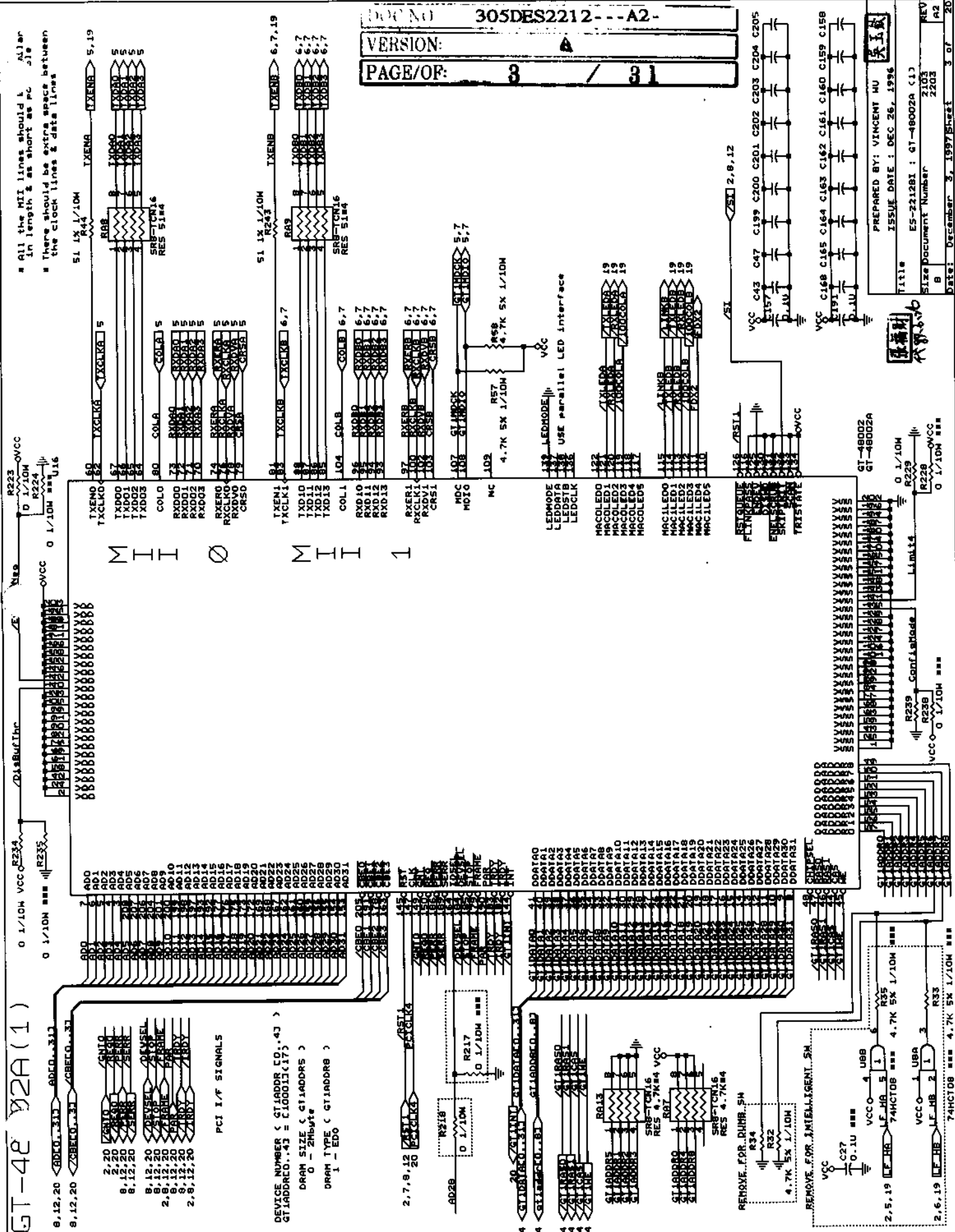
Be careful of the placement of M1, M2  
Don't put M1, M2 in front of the fans



D-Link <sup>®</sup> Corp.		Approved: [Signature]	Prepared by: VINCENT MU	15.2 X 11.7
DOC. NO.: 305DES2212-A2-		Checked: [Signature]	ISSUE DATE: DEC 26, 1996	
		Version: A	Title: ES-2212BI : POWER/FAN CONN. & SYS CLOCK	
			Size Document Number: 2103	
			REV: 2203	
			Date: December 3, 1997	1 of 20



- All the MII lines should be as short as possible
- There should be extra space between the clock lines & data lines



3 / 31

Size	Document Number	REV
B	2103	A2
	2203	
Date:	December 3, 1997	Sheet 3 of 20

1

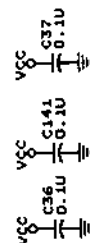
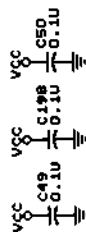
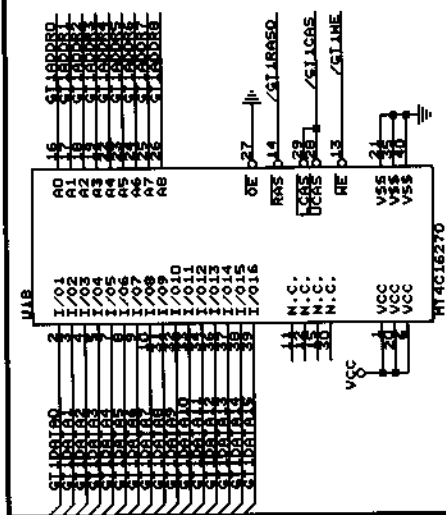
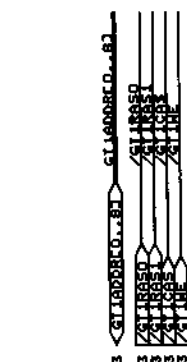
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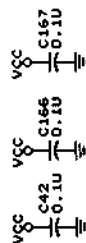
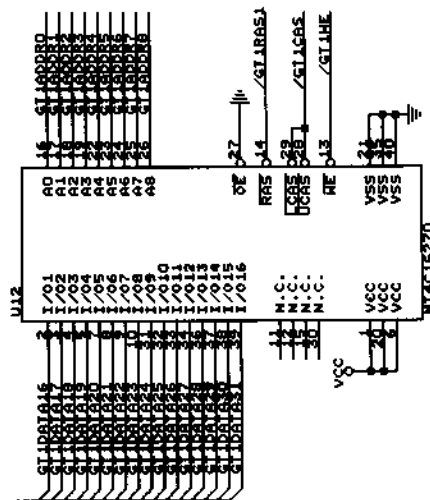
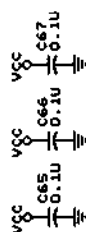
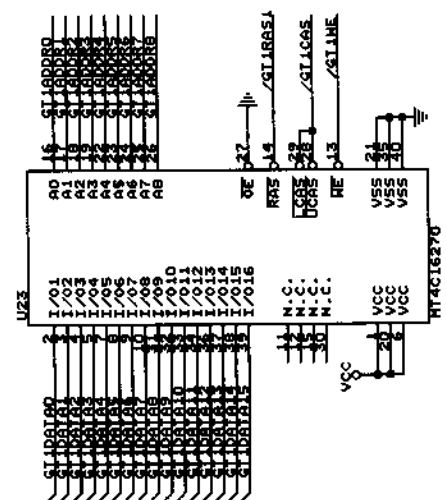
4.7K 5

2.

SECRET



USE 2M BYTE MEMORY.  
FOR GT-48002CA)  
MEMORY IS 60ns EDO RAM



# D-Link

**Approved:** \_\_\_\_\_  
**Checked:** \_\_\_\_\_

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PREPARED BY: VINCENT WU  
ISSUE DATE : DEC 26, 1995

ES-2212BI : DRAM FOR GT-48002A (1)

DOC. NO.: 305DES2212--A2-

Size Document Number	2103	REV
B	2203	AZ
Date: December 3, 1997 Sheet 4 of 20		



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PHY MODE ENABLE
EN/DECODER ENABLE
SCRAMBLER ENABLE
IOBASE-TX ENABLE
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REGRO--17 = 11 C100M. DISABLE JOBASE-T LINK TEST

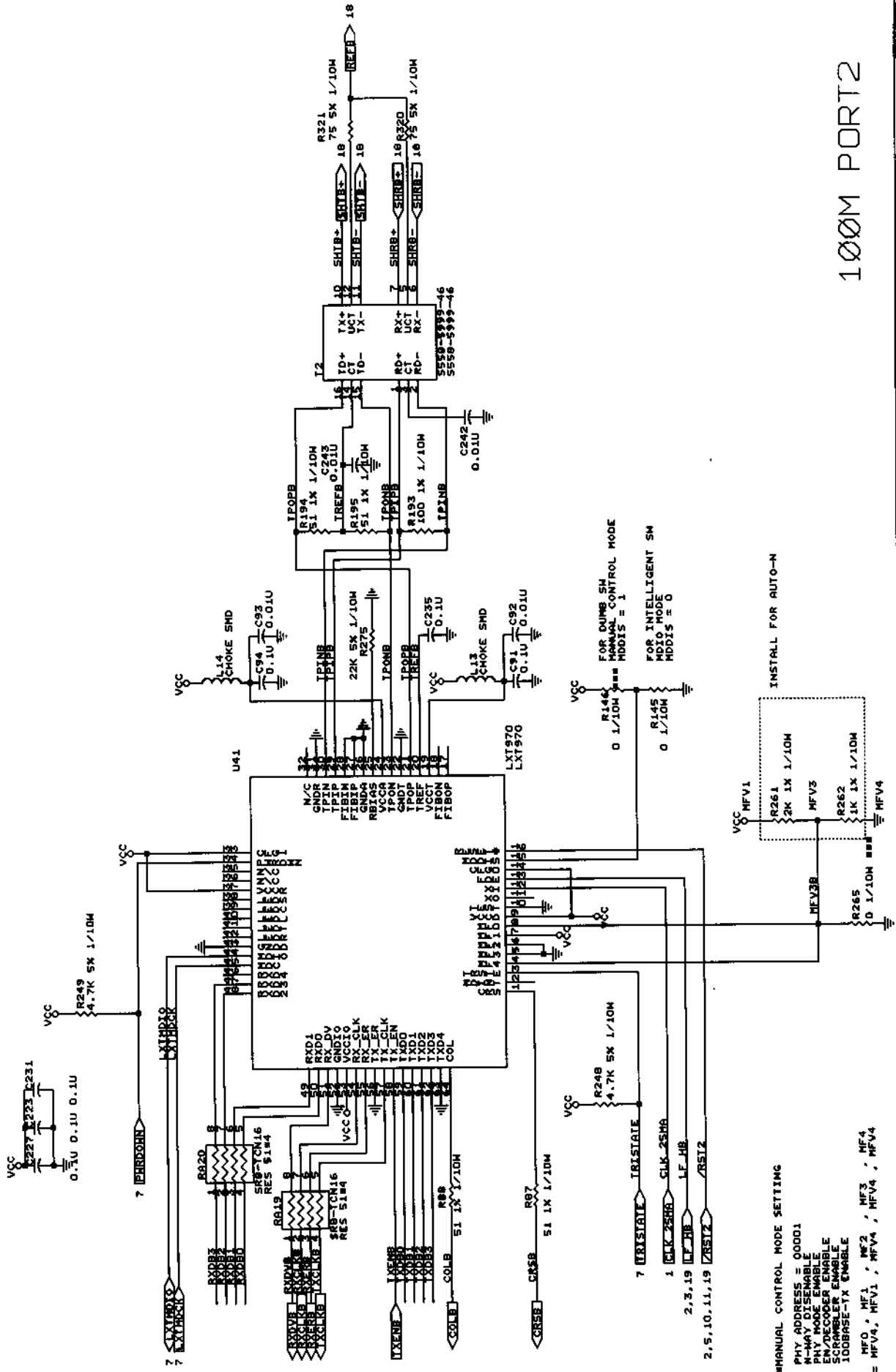
## 100M PORT 1

**D-Link®**

Approved: 張福財  
Prepared by: VINCENT WU  
Rising Sun  
Date: 2004

Checked:	張國財	Title	ES-221281 : 100H PORT1 OKT	ISSUE DATE : DEC 28, 1978
Version:	A	Size	Document Number	REV
		B	2103	1
		D	2203	2
		Date	December 3, 1997	Sheet 5 of 2

3.7 RXDBE0..31  
3.7 TXDBE0..31



100M PORT2

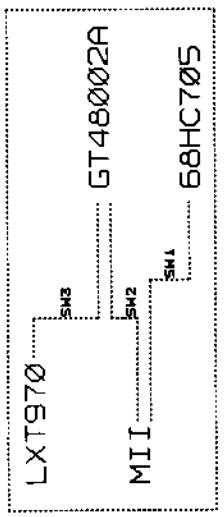
#MANUAL CONTROL MODE SETTING  
PHY ADDRESS = 00001  
PHY MODE = 100M  
PHY MODE ENABLE  
EN/DECOODER ENABLE  
SCRAMBLER ENABLE  
100BASE-TX ENABLE  
MF0, MF1, MF2, MF3, MF4  
= MFV4, MFV1, MFV4, MFV4, MFV4

CFGE0..13 = 11 (100M, DISABLE 10BASE-T LINK TEST)

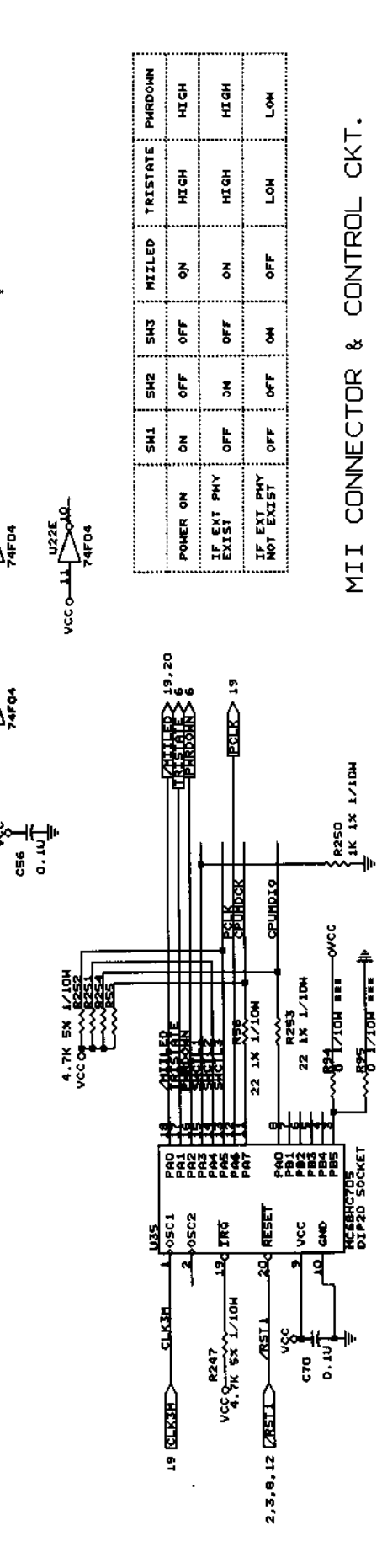
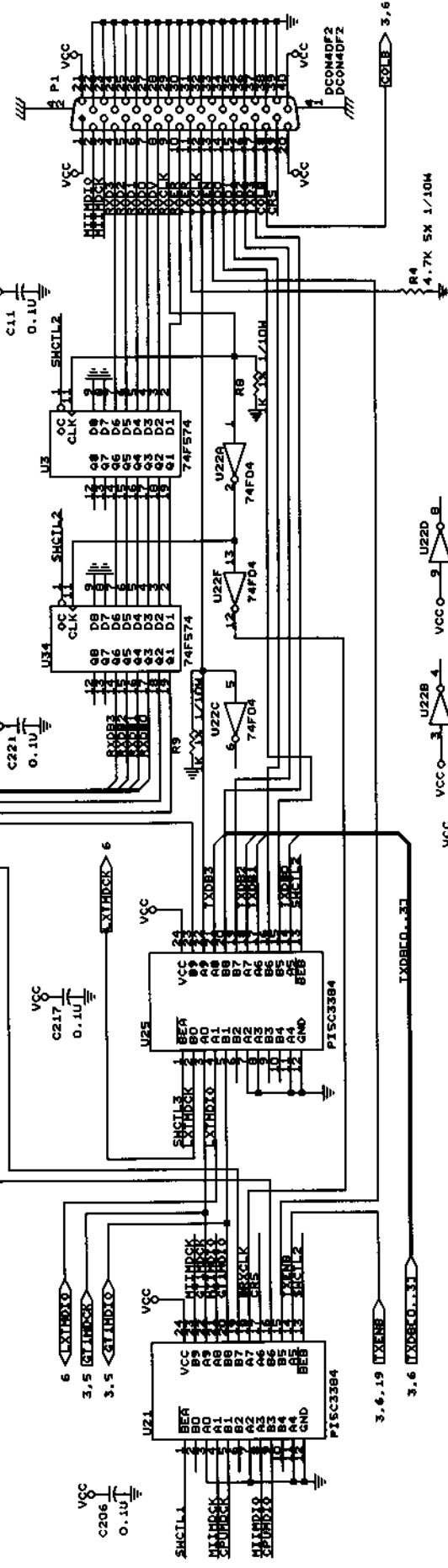
Approved:		Prepared by: VINCENT MU	
Checked:		Issue Date: DEC 26, 1996	
Title: 100M PORT2		ES-2212BI : 100M PORT2 CKT	
Version: A		Size Document Number: 2103	
DOC. NO.: 305DES2212--A2-		Date: December 3, 1997 Sheet 6 of 20	

**D-Link** Corp.





# 40 PINS MII CONNECTOR



SM1	SM2	SM3	MILED	TRISTATE	PHRDOWN
POWER ON	ON	OFF	ON	HIGH	HIGH
IF EXT PHY EXIST	OFF	ON	ON	HIGH	HIGH
IF EXT PHY NOT EXIST	OFF	OFF	ON	LOW	LOW

## 40 PINS MII CONNECTOR & CONTROL CKT.

**D-Link**  
Corp.

FOR READING THE EXTERNAL PHY  
MICRO-P FOR PROCESSING EXTERNAL 100M PHY

Approved: 張福財

Checked: 張福財

Doc. No.: 305DES2212--A2-

Version: A

Prepared By: VINCENT MU 吳玉斌

Issue Date: DEC 26, 1996

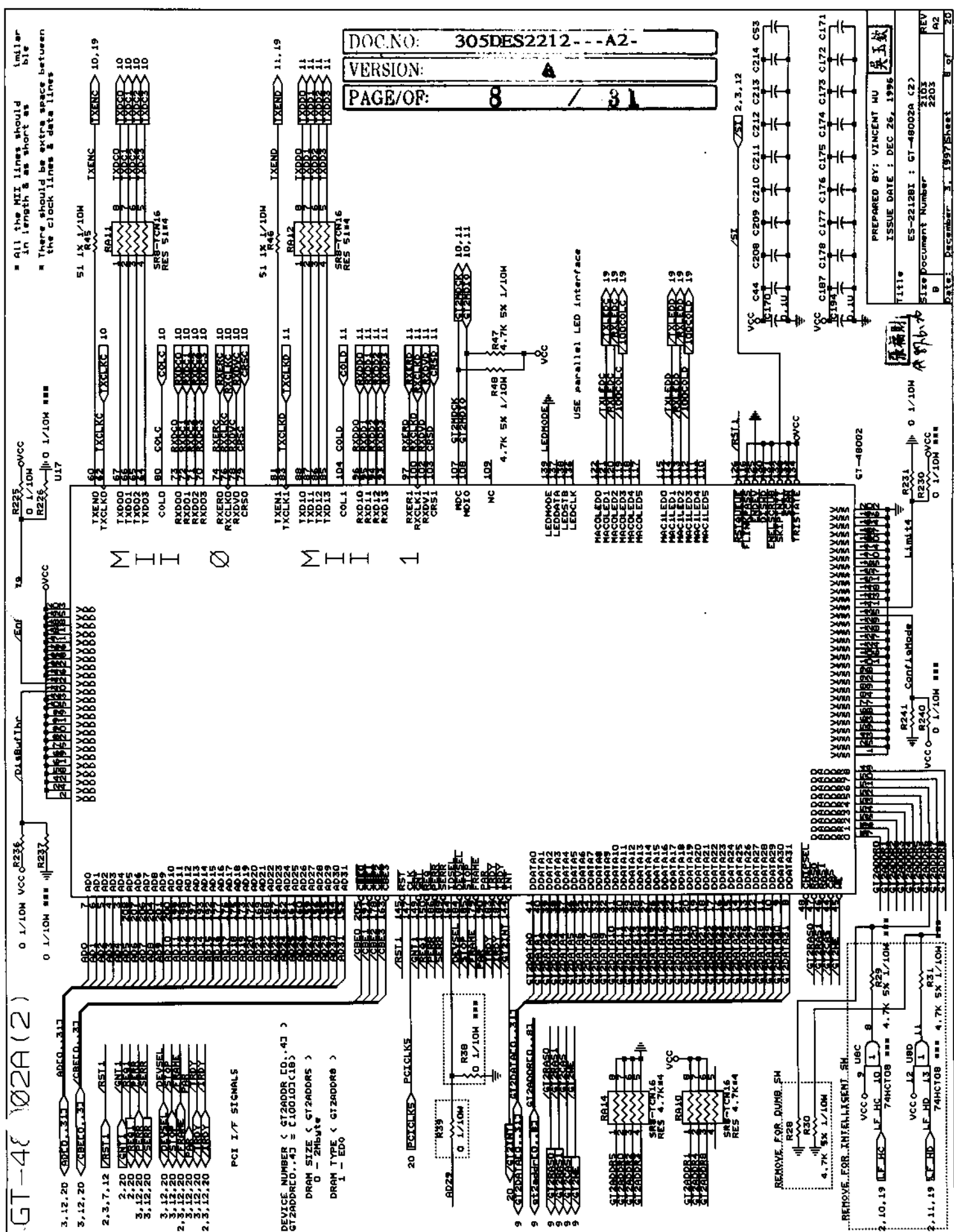
Title: ES-2212BI : 100M MII CONN. & CONTROL CKT

Size Document Number: 2103 2203

Date: December 3, 1997

Sheet: 7 of 20

GT-4802A(2)





DOC.NO: 305DES2212---A2-  
VERSION: A  
PAGE/OF: 8 / 31

PREPARED BY: VINCENT HU  
ISSUE DATE: DEC 26, 1996  
Title: ES-2212BI : GT-4802A (2)  
Size Document Number: 2203  
REV: A2  
Date: December 31, 1997 Sheet 8 of 20

GT2DATA.C...317



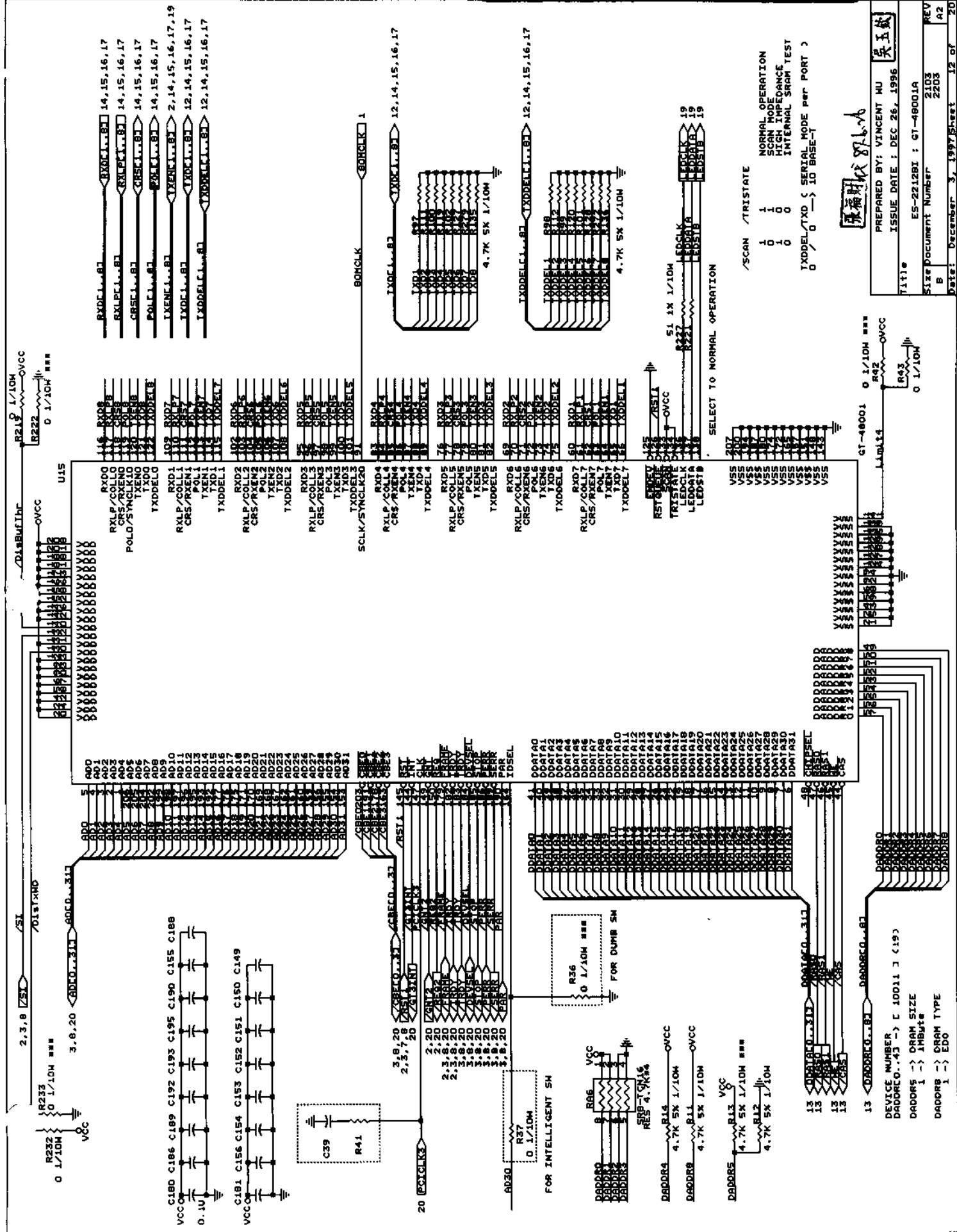
# D-Link®

Approved:  Prepared by: VINCENT HU  
 Issue Date: DEC 26, 1996  
 吳玉欽

Checked:	張福財	Title	ES-221281 : DRAW FOR G1-48002A (2)	REV	A2
		Size	Document Number	2103	A2
		Version:	B	2203	
		Date:	December 3, 1997	Sheet	9 of 2







康福財收 89.6.6

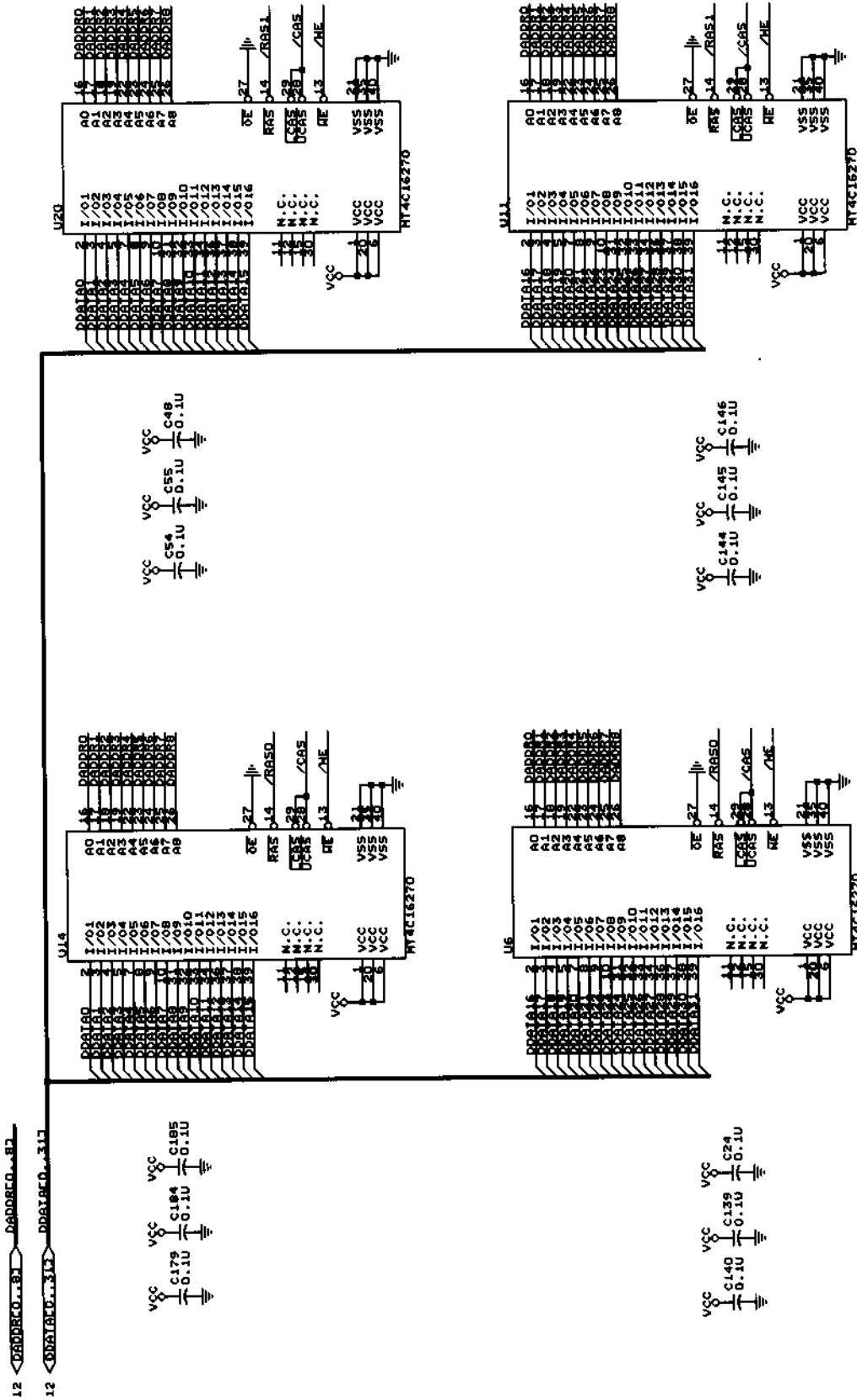
PREPARED BY: VINCENT HU  
 ISSUE DATE: DEC 26, 1996  
 ES-2212BI : GT-48001A  
 Size Document Number 2103  
 REV A2  
 Date: December 3, 1997 Sheet 12 of 20

SCAN /TRISTATE  
 1 1 NORMAL OPERATION  
 0 1 SCAN MODE  
 0 0 HIGH IMPEDANCE  
 0 0 INTERNAL SRAM TEST  
 TXDDSEL/TXD 5 SERIAL MODE per PORT 3  
 0 / 0 -> 10 BASE-T

DEVICE NUMBER  
 DADDR0..43 -> C 10011 3 (19)  
 DADDR5 -> ORAM SIZE  
 1 -> 1MByte  
 DADDR8 -> ORAM TYPE  
 1 -> EDO

12	RAST	RAST
12	RAST	RAST
12	CAS	CAS
12	ME	ME

FOR GT-48001A



USE 1M BYTE MEMORY.  
FOR GT-48001(A)  
MEMORY IS 60ns EDO RAM

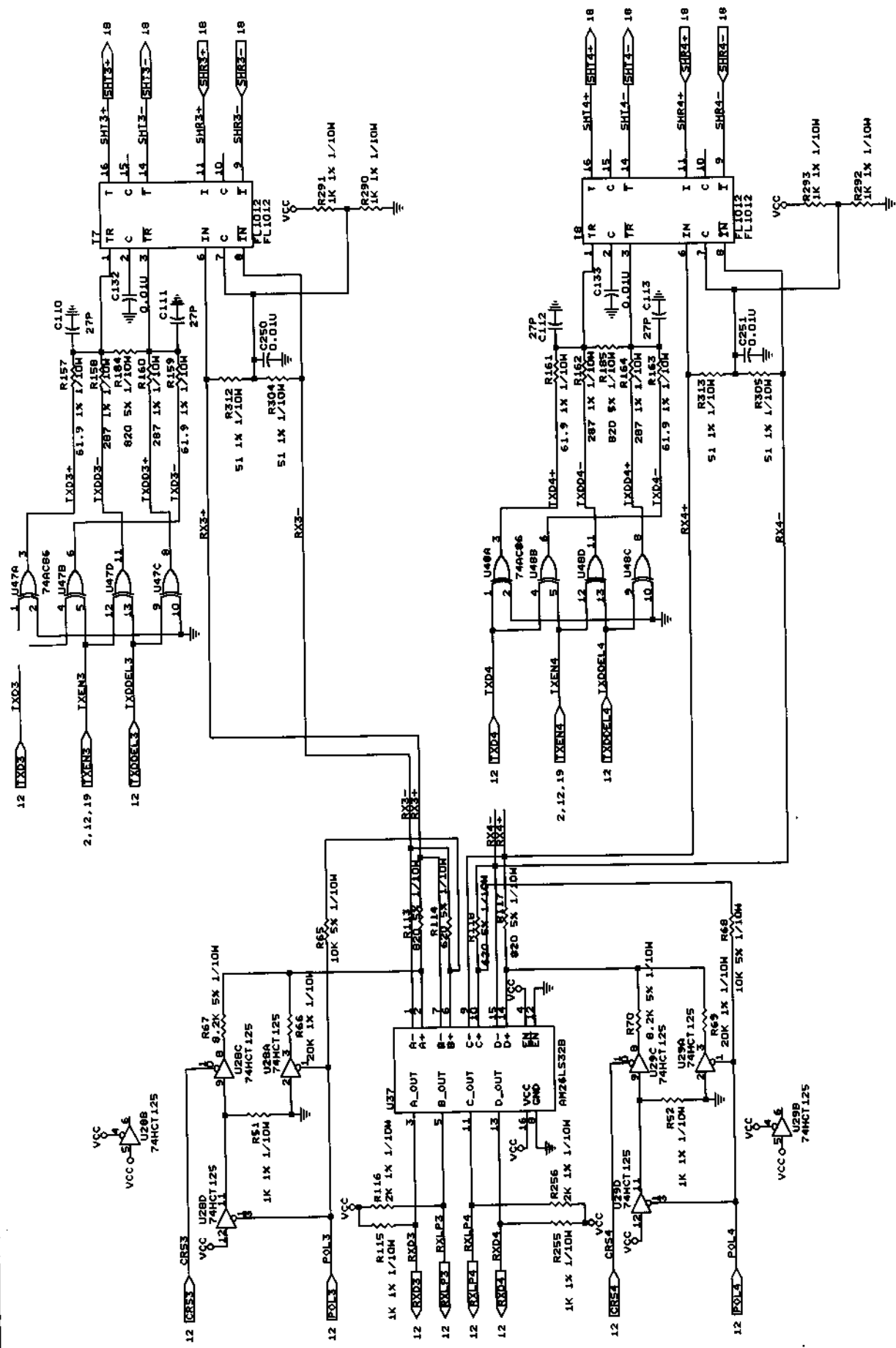
PREPARED BY: VINCENT HU	吳玉斌
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ES-221281 : DRAM FOR GT-48001A

DWG. NO.:	305DES2212---A2-
Version:	A
Size	B
Document Number	2103 2203
Date	December 7, 1997
Sheet	1 of 20
REV	A2

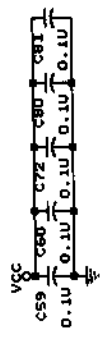


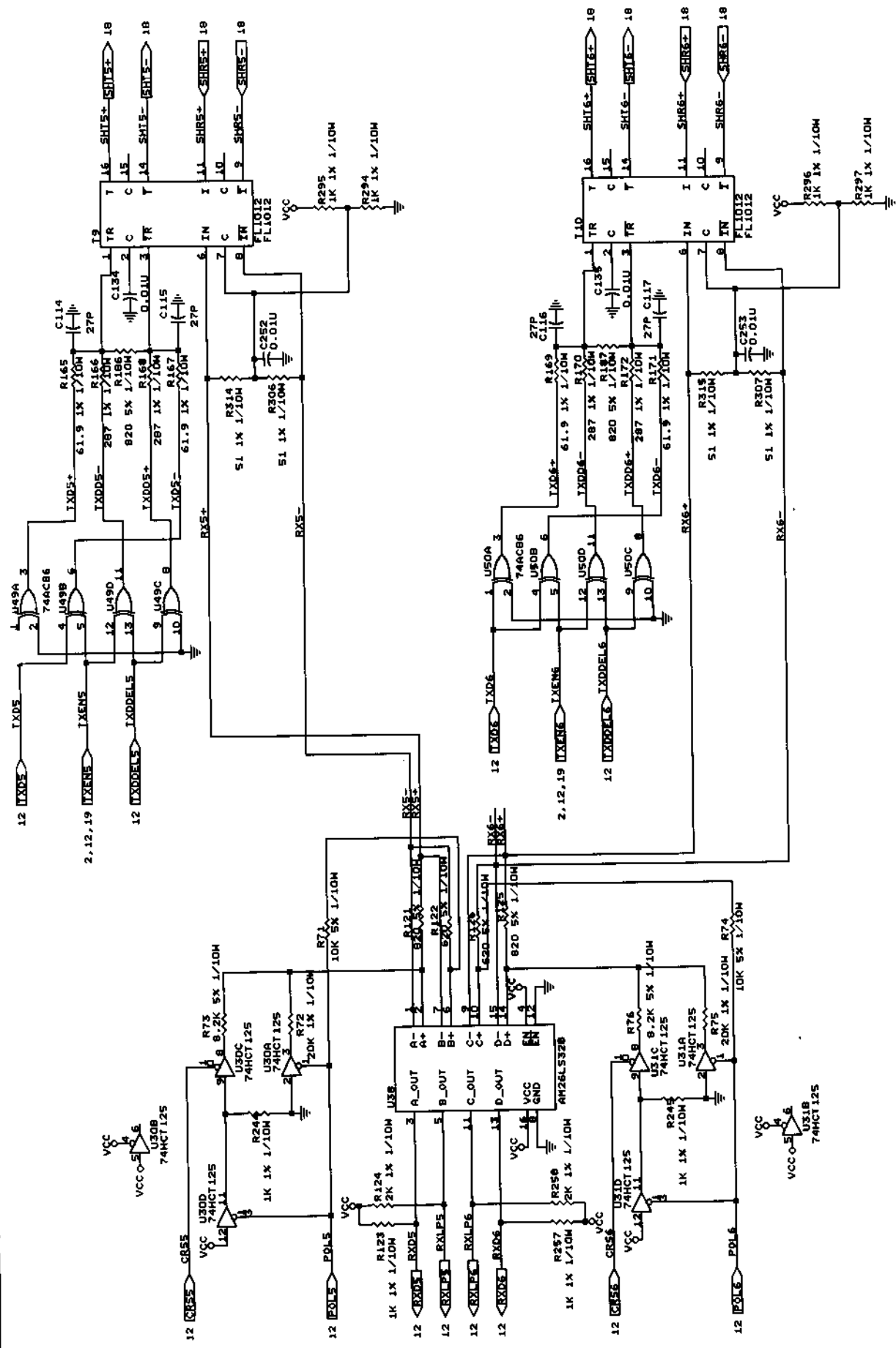




10M PORT7 & PORT8

<b>D-Link</b> Corp.		Approved: 張福財	Checked: 張福財	Version: A	Doc. No.: 305DES2212---A2-
Title: 張福財		Prepared by: VINCENT HU		Issue Date: DEC 26, 1996	
Rev: 2103		Title: ES-2212B1: 10M PORT7 & PORT8 CKT		Size: 2203	
Rev: A2		Title: 張福財		Issue Date: December 3, 1997	
Rev: 2103		Title: 張福財		Issue Date: December 3, 1997	
Rev: A2		Title: 張福財		Issue Date: December 3, 1997	





10M PORT9 & PORT10

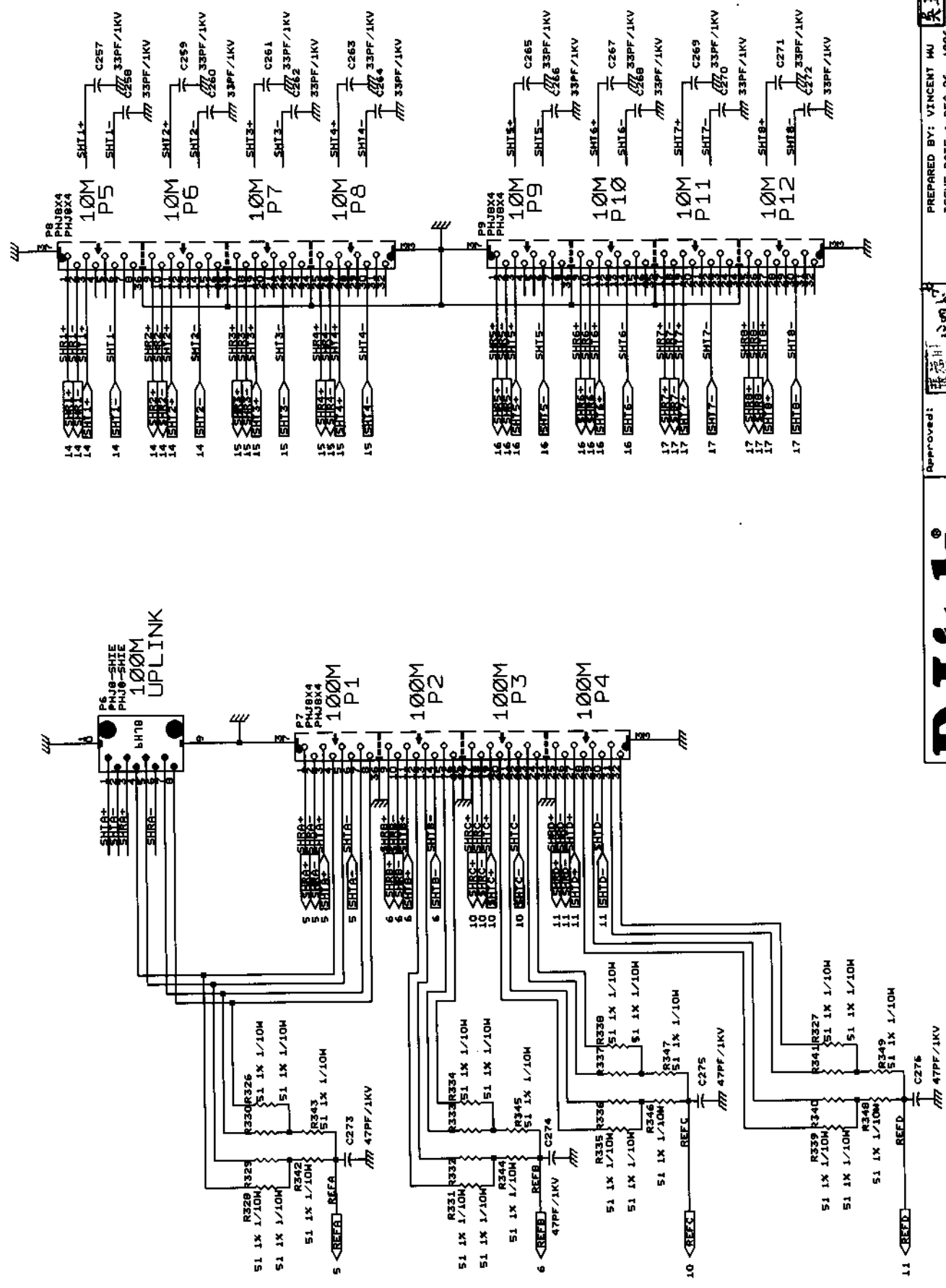
<b>D-Link</b> Corp.		Approved: 張福財	Checked: 張福財	ES-2212B1 : 10M PORT9 & PORT10 CNT	REV 2103
DOC. NO.: 305DES2212--A2-		Version: A		Size Document Number	A2
		Prepared BY: VINCENT HU		Issue Date : DEC 26, 1996	REV 2103
				File: December 3, 1997/Sheet 16 of 20	A2

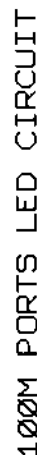


# 100M & 10M PHONE JACKS

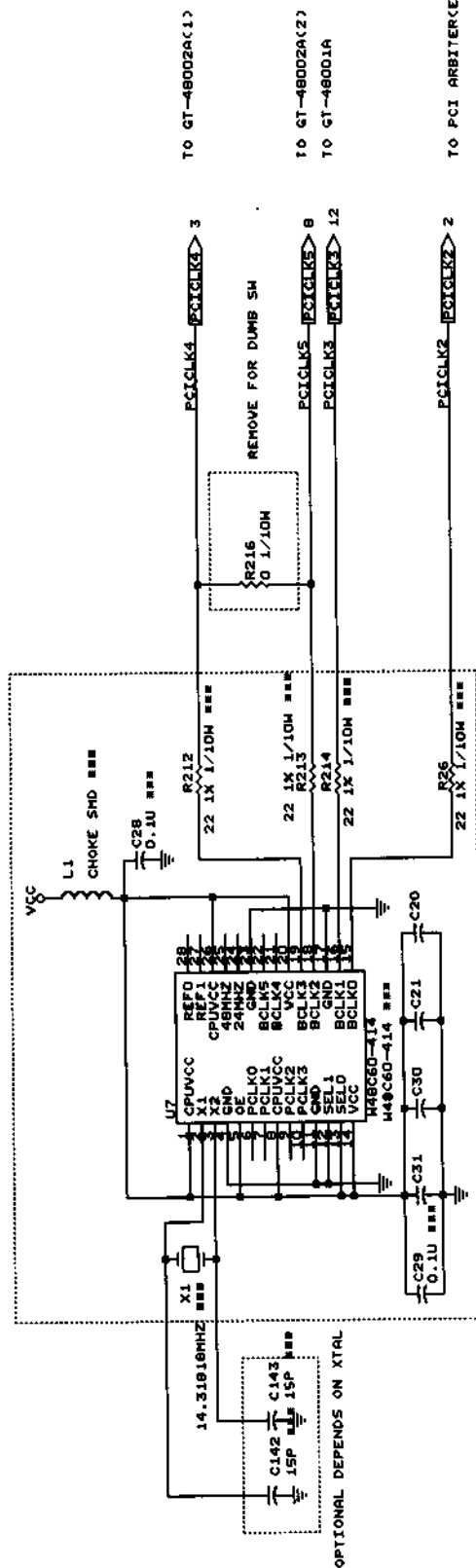
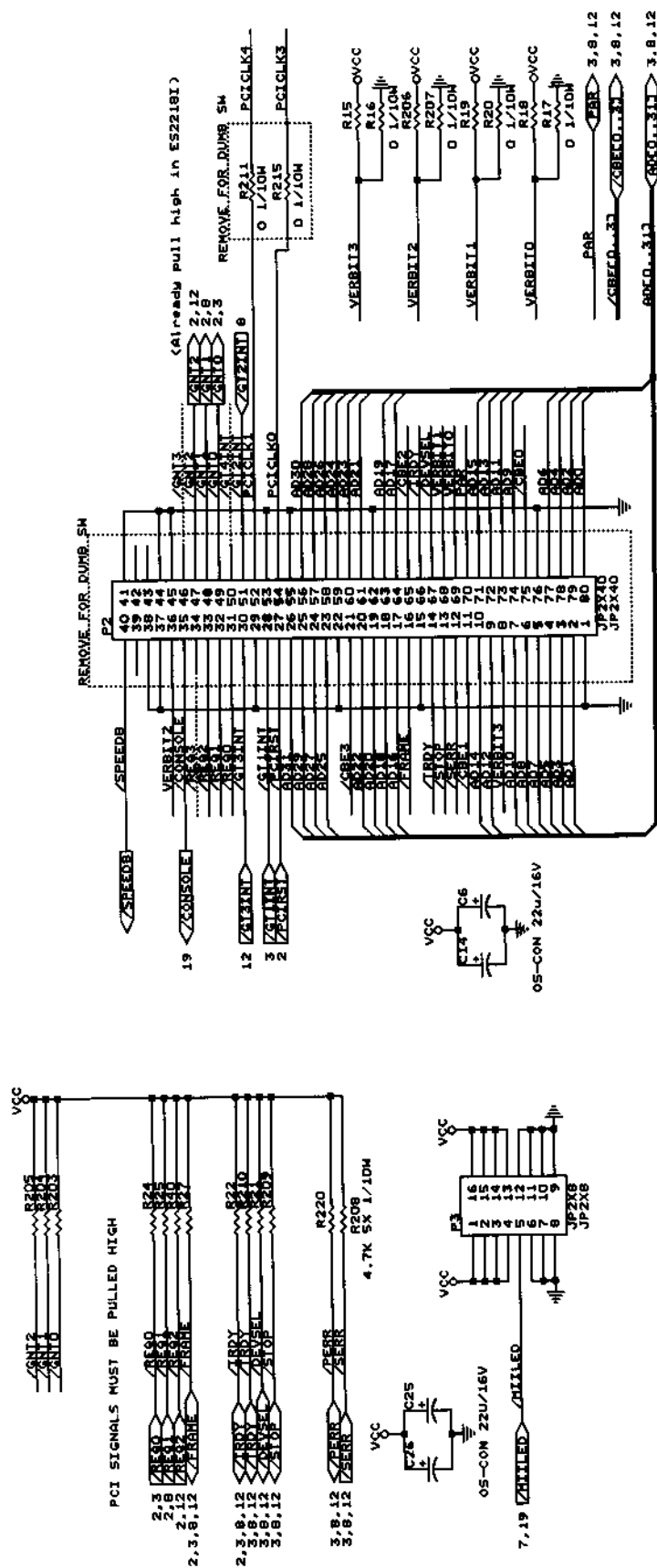


Approved: 張志輝  
Checked: 張志明  
Version: A  
Title: ES-2212BI : PHONE JACKS  
Doc. No.: 305DES2212--A2-  
Prepared By: VINCENT HU  
Issue Date: DEC 26, 1996  
Size: Document Number 2103  
Rev: 2203  
Date: December 3, 1997 Sheet 18 of 20





26, 19



\*\*\*\*\*  
 REMOVE FOR INTELLIGENT SW

PCI CLOCK (33M) GENERATION  
FOR DUMB SW

# D-Link

DOC. NO.: 305DFS2212---A2-

**Version:**

Title	Accession Number	Accession Date	Accession Time	Accession Location	Accession Status	Accession Remarks
ES-22129T : B2B COMM & BCT CLCKS						

Size Document Number

B	Date: December 3,
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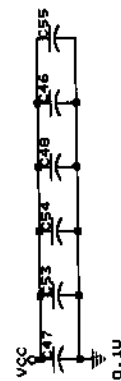
PREPARED BY: VINCENT HU  
ISSUE DATE : DEC 26, 1999

**ISSUE DATE : DEC 26, 1996**

吳玉菴

B	4203	AZ
Date: December 3, 1997 Sheet 20 of 20		

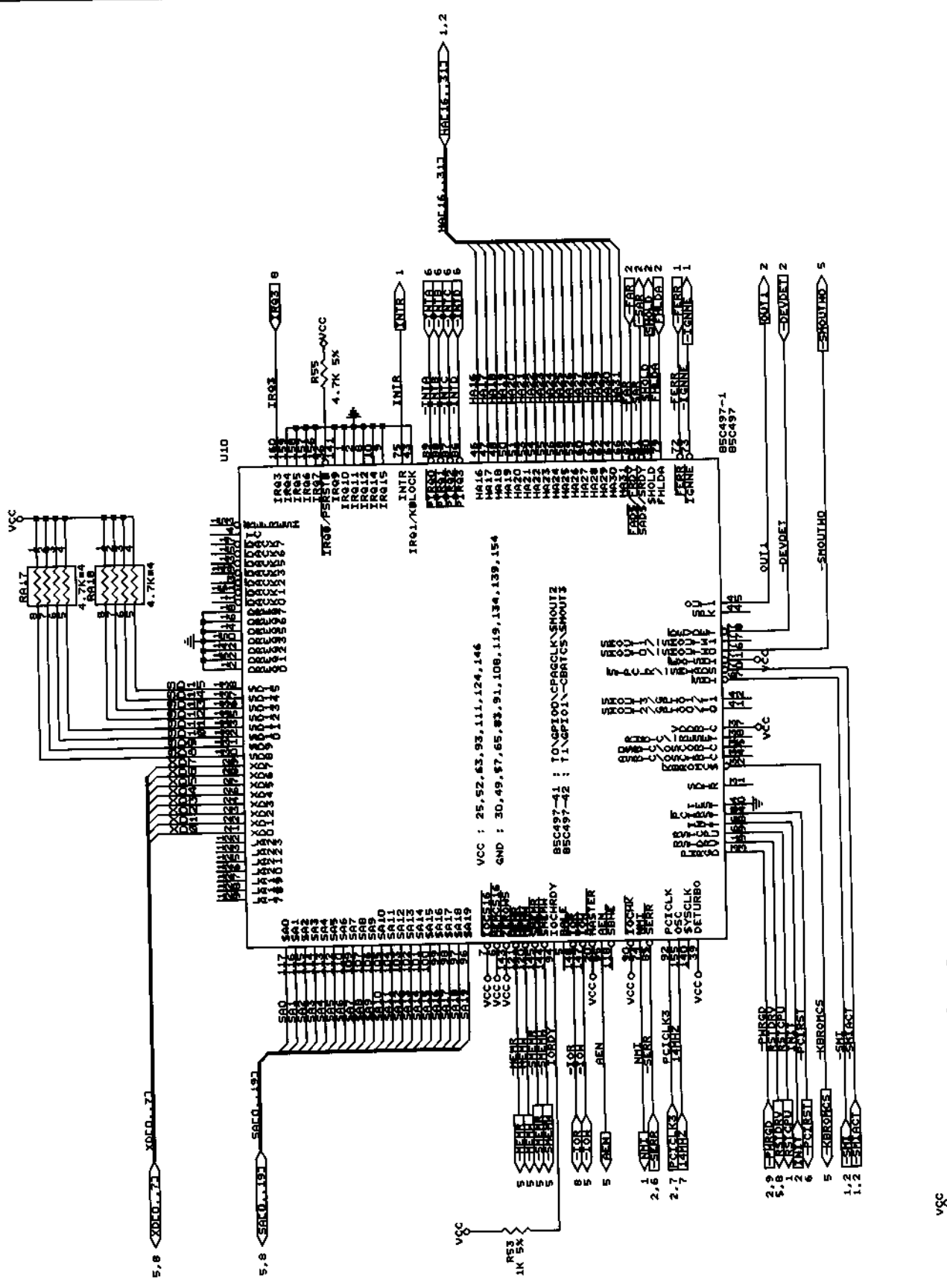




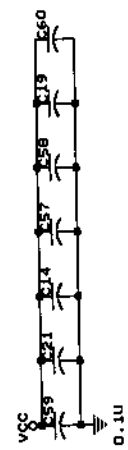
ed by: Vincent MU  
Date: May 15, 1997  
E5-2210I 515

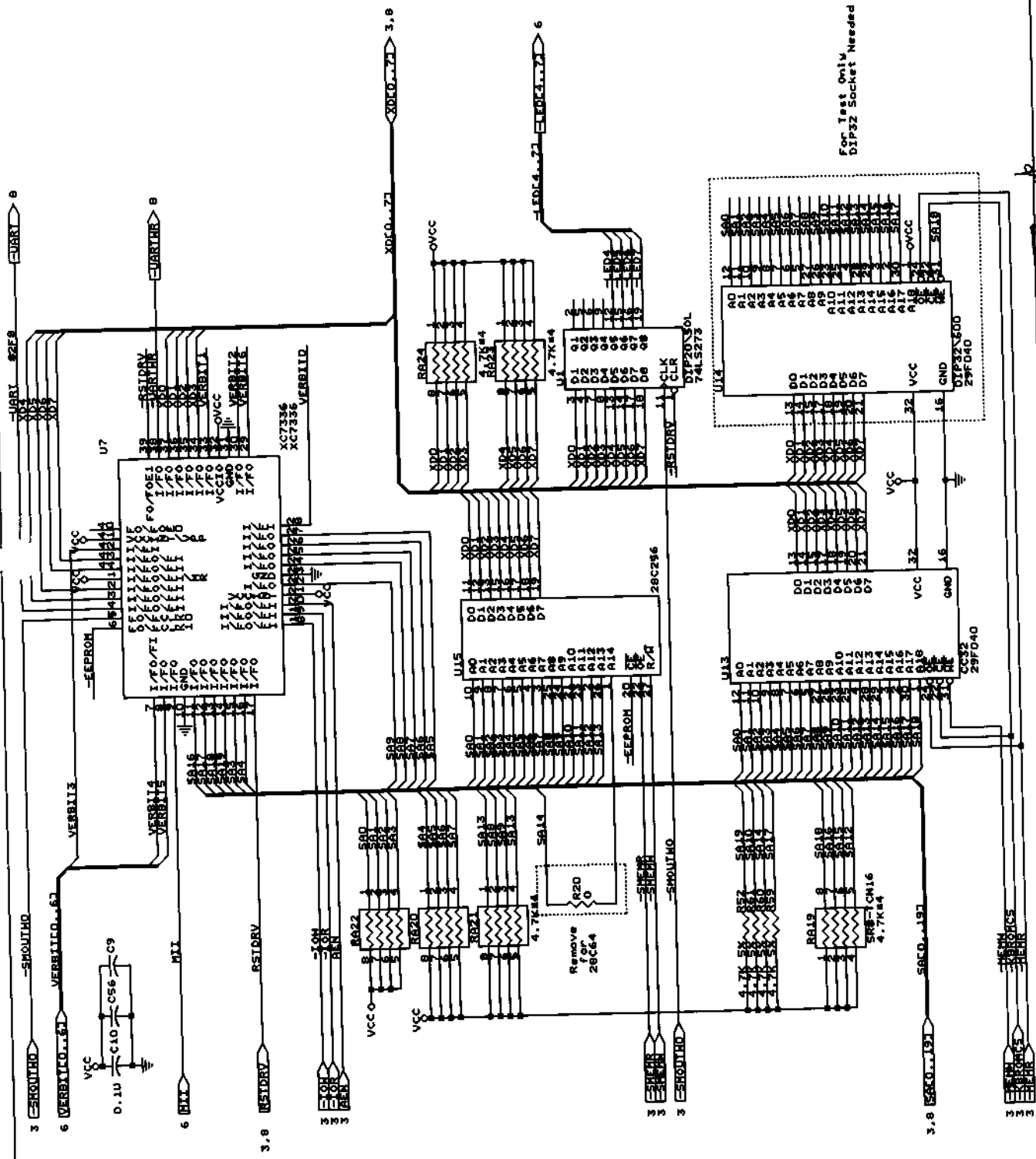
2 of 2





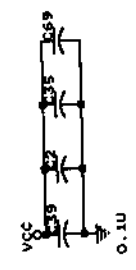
<b>D-Link</b> Corp.		Approved:		Prepared by: Vincent HU	
Doc. No.: 305DES2212---A2-		Checked:		Issued Date: May 15, 1997	
Version: A		Title: ES-22101		Size: 2102	
Date: JULY 15, 1997		Size Document Number: 2202		REV: A1	





For Test Only  
DIP32 Socket Needed

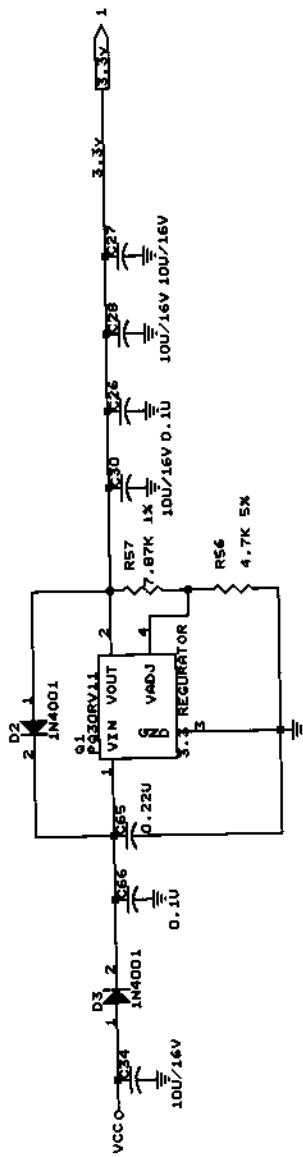
Approved: 张福财 张福财  
Checked: 张福财 张福财  
Version: A  
DOC. NO.: 305DES2212---A2-  
Prepared by: Vincent HU  
Issued Date: May 15, 1997  
Title: ES-22181 ROM & EEPROM & LED R/G & DECODER  
Size: Document Number  
REV: 2102  
A1  
Date: JULY 15, 1997 Sheet 5 of 5



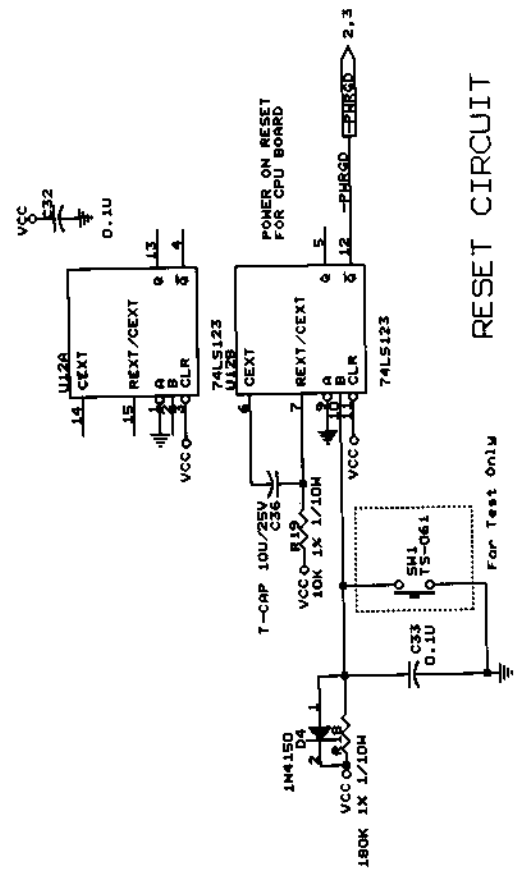
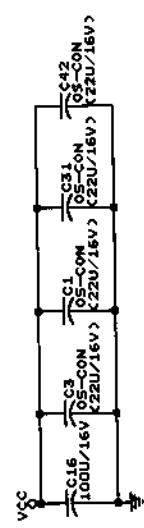








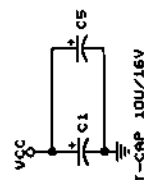
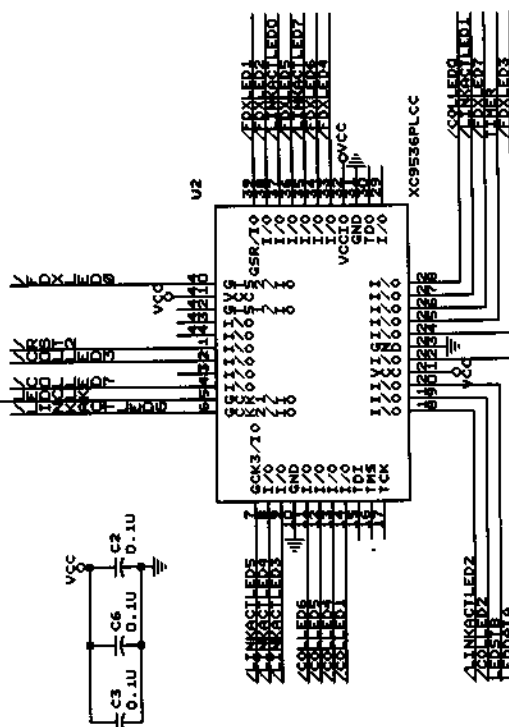
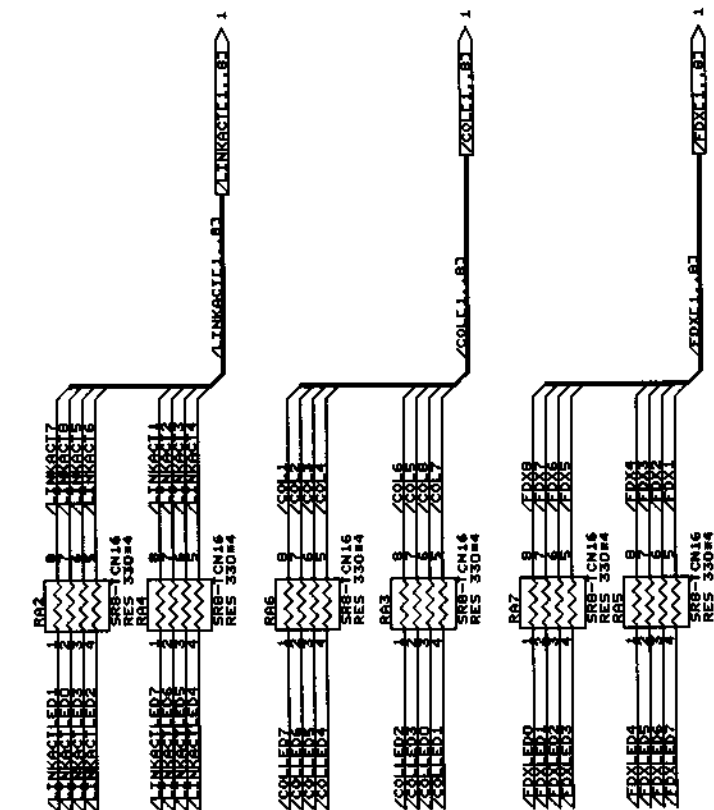
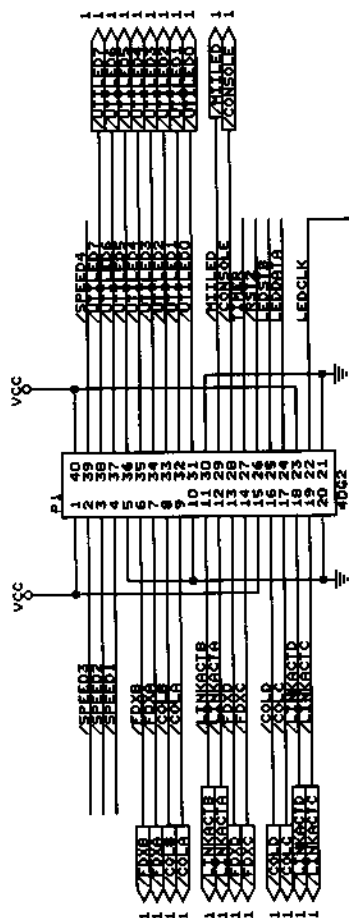
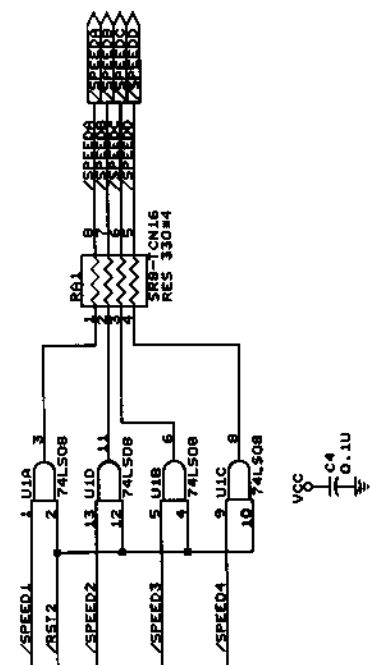
5V -> 3.3V POWER CONVERSION



RESET CIRCUIT

<h1 style="margin: 0;">D-Link</h1> <p style="margin: 0;">Doc. No.: 305DES2212--A2-</p>		Approved:	Prepared by: Vincent MU	<div style="border: 1px solid black; padding: 2px;">             吳玉斌           </div>
		Checked:	Issued Date: MAY 15, 1997	
		Version: A	Title: ES-22181 POWER & RESET	REV
			Size Document Number	2102
			Date: JULY 15, 1997	Sheet 5 of 5





Approved: [Signature]		Prepared by: VINCENT MU		15.2 X 11.7	
Checked: [Signature]		Issue Date: JULY 7, 1997		REV A1	
Title: ES-2212L : LED CABLE CONN. & DECODE CKT		Version: A		Date: AUGUST 6, 1997 Sheet 2 of 2	
Doc. No.: 305DES2212-...A2-		Size: 2103		REV A1	

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