



DOC NO. 305DES18--B1-

VERSION

PAGE/OF 0 / 33

生效日期: 87. 4. 17

DES 818 Rev. B1

1000

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APPROVED	CHECKED	DEPARTMENT	PREPARED
30 李林 2010/1/10	X	卓裕文	203 P. 114

卓裕文

DES-818 TOP-PCB REV. B1

DES-818's UP_PCB

PC1_CLOCK.DIPSWICH	SI48001CMIL
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C_BEMCO..33	C_BEMCO..33
TXENCO..73	TXENCO..73
REQ#2	REQ#2
GNT#2	GNT#2
PERR#	PERR#
SERR#	SERR#
DEVSEL#	DEVSEL#
STOP#	STOP#
FRAME#	FRAME#
PAR#	PAR#
TRDY#	TRDY#
IRDY#	IRDY#
SI	SI
BMCLK	BMCLK
PC1CLK1	PC1CLK1
RST#1	RST#1
21_PC1.SCH	21_MMC.SCH

EDM, D-Link®		Approved: <i>Charles R. [Signature]</i>	Prepared: POLLY PAN
File Name: 21_818.SCH		Chief Engineer: <i>21/2</i>	Issued Date: [Blank]
Doc. No.: 305DES818--B1-	Version: A	Size Document Number: DES-818's TOP PCB	REV B1
		Date: August 26, 1997	Sheet 1 of 12

005810 UP PCB : FEMOLE



Prepared by : POLLY PAN

Issued Date :	File
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005-0187, TOP PCB

Size Document Number	B	01A-00-0000-M30
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Date: September 23, 1997 Sheet 2

DOC- NO-: 005070010

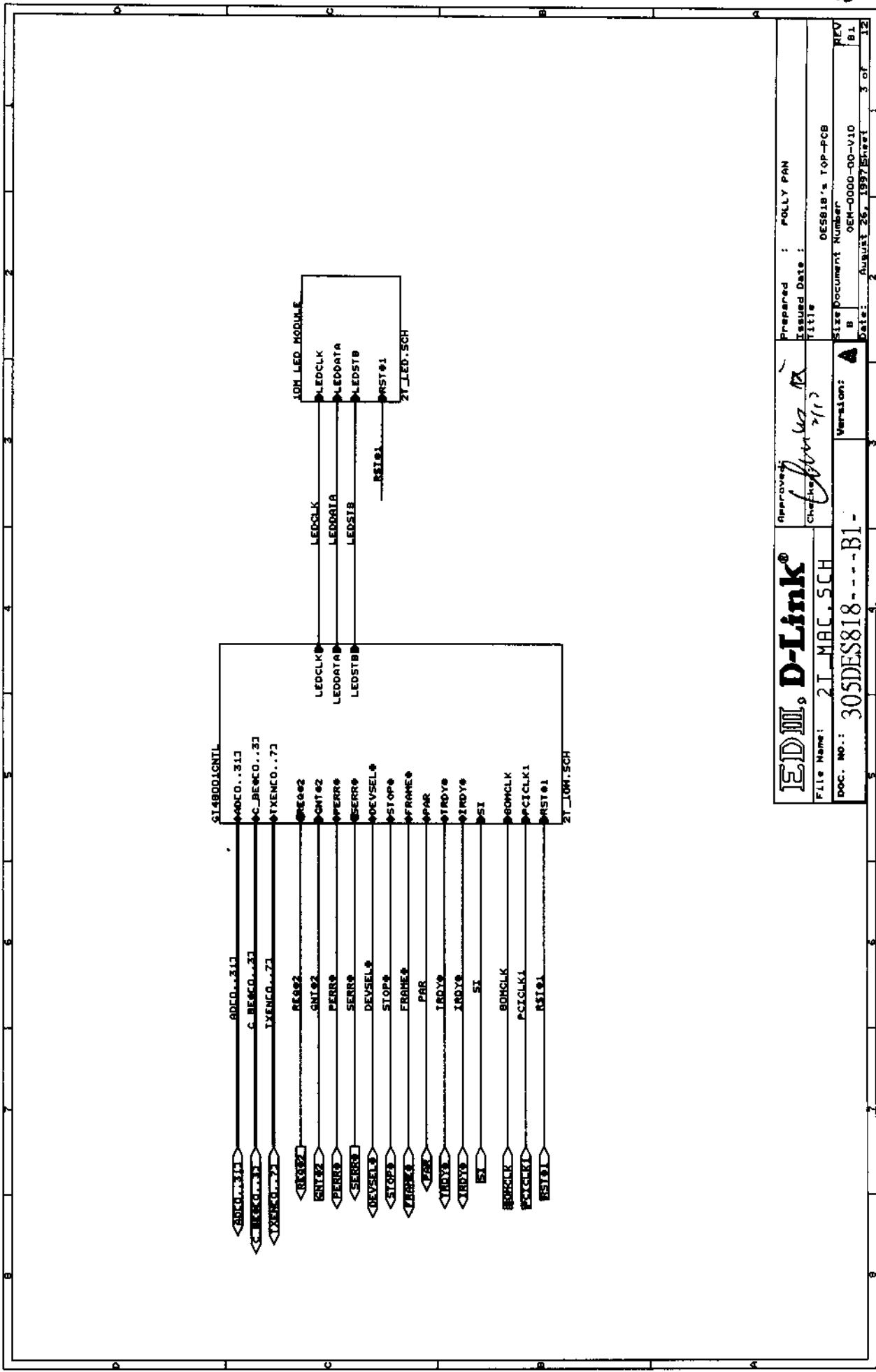
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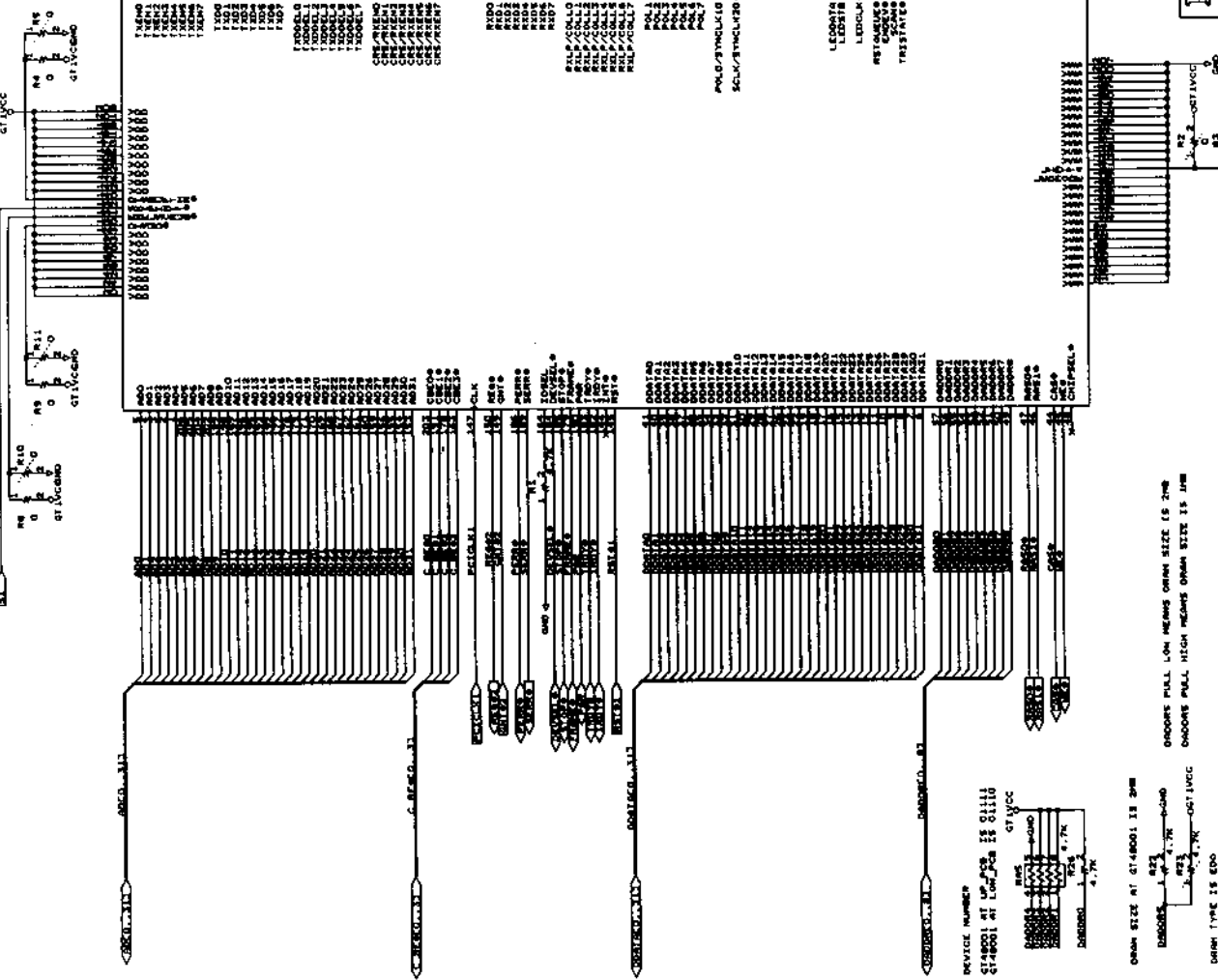
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DOC. NO.: 305DES818---B1-

Size Document Number: DES818's TOP-PCB
B
Date: August 25, 1997 Sheet 3 of 12

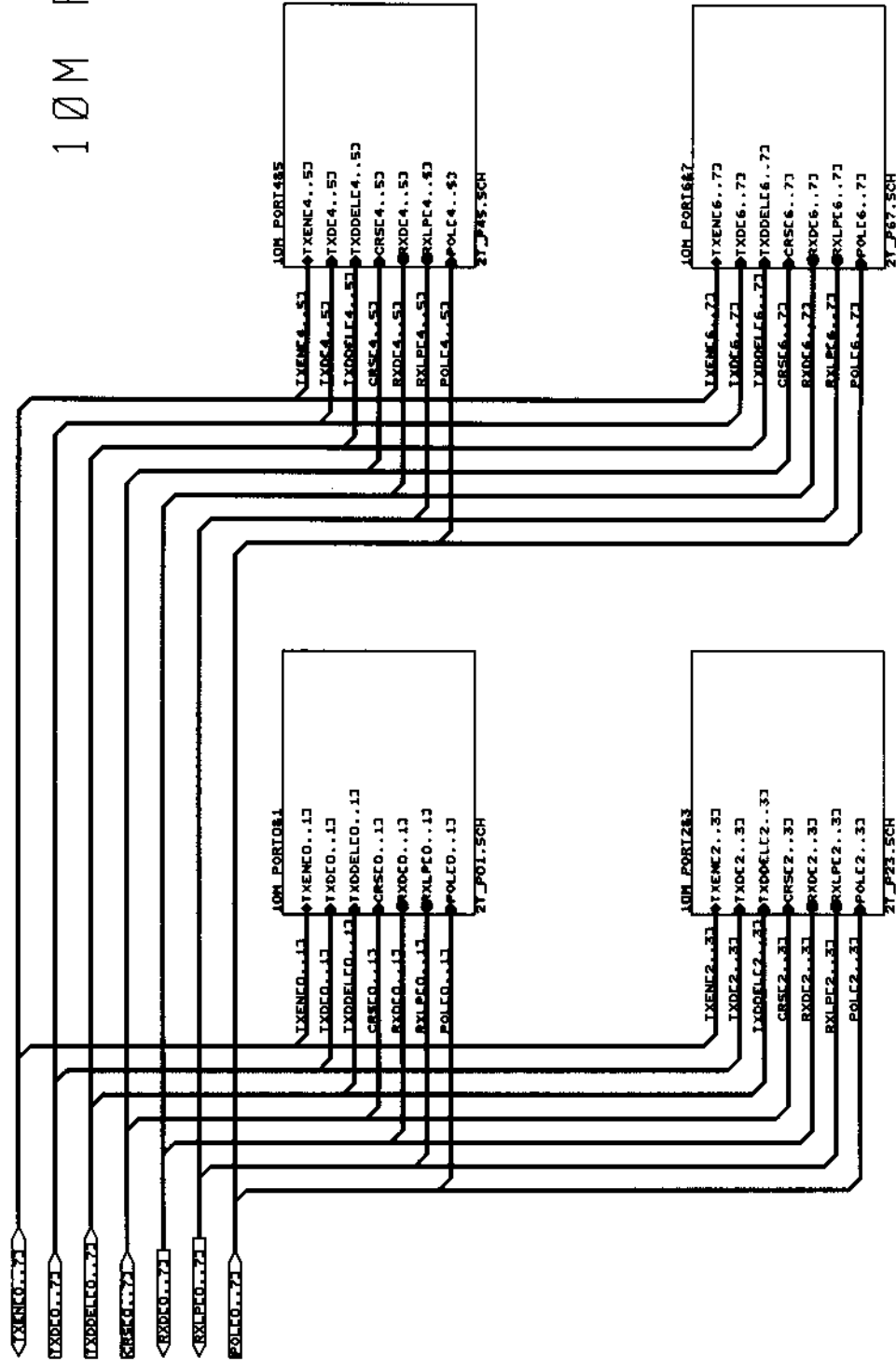
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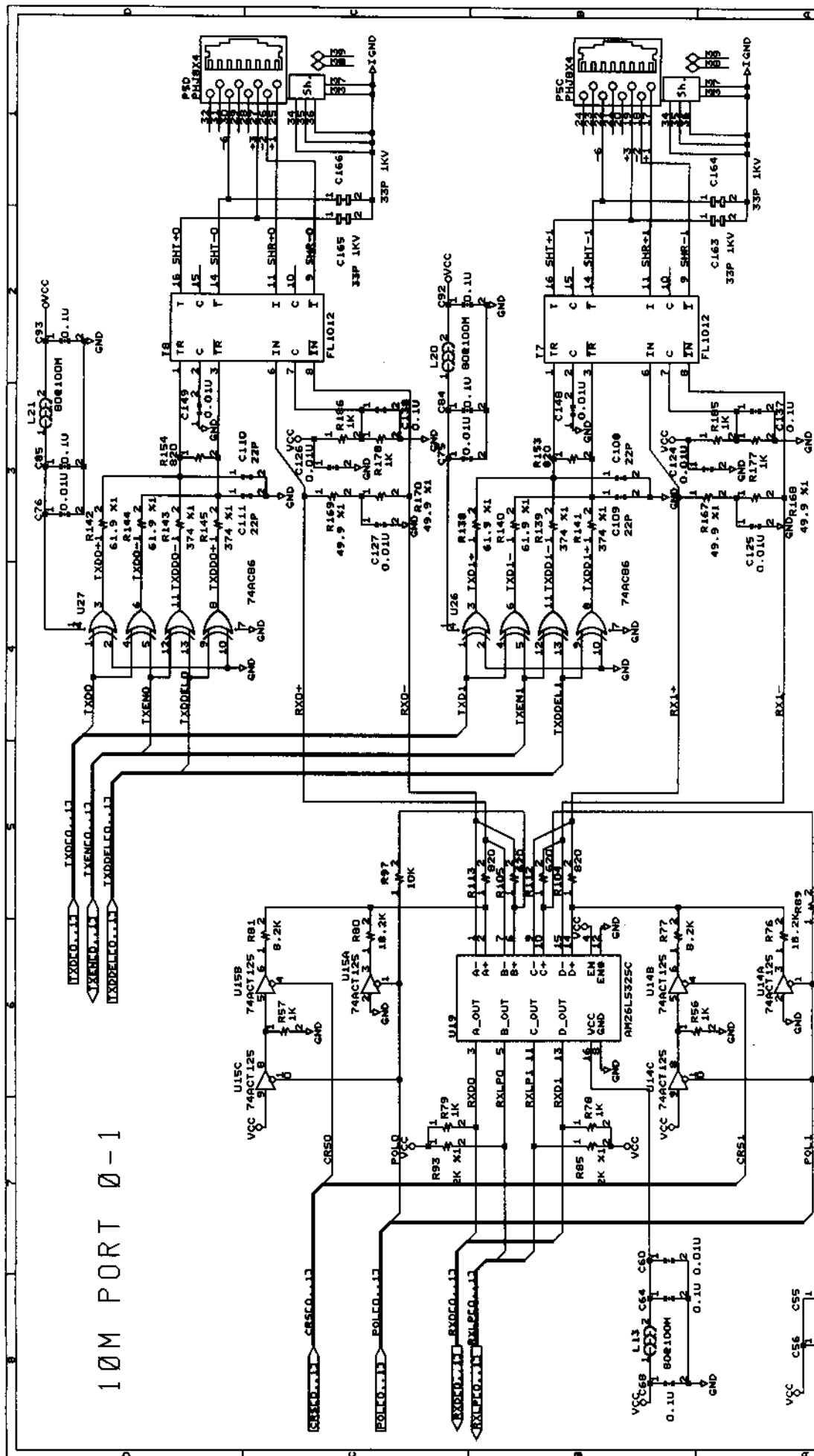
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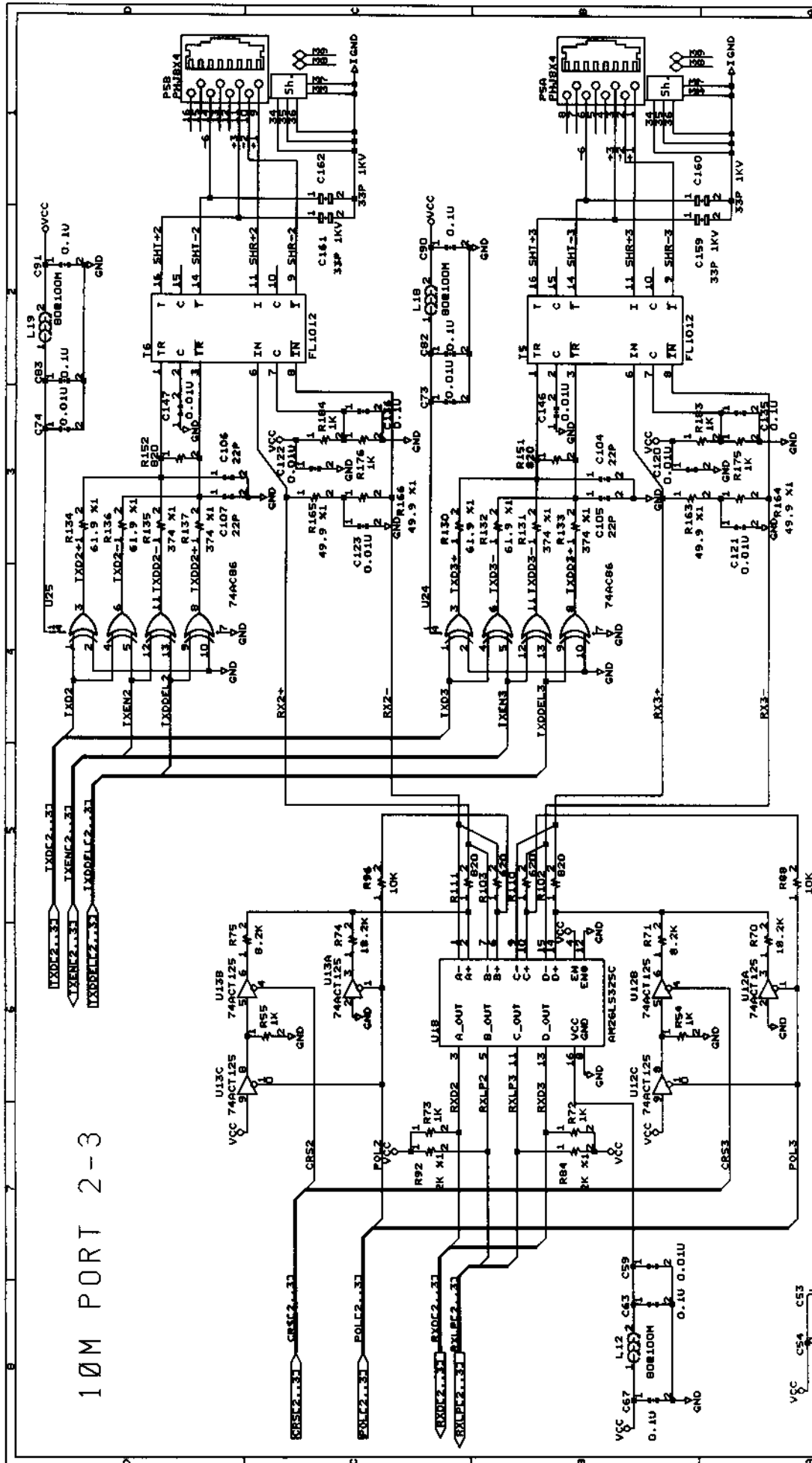
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Date: June 19, 1997 Sheet 7 of 12

File Name: 2T_818RX.SCH
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Version: A



10M PORT 2-3



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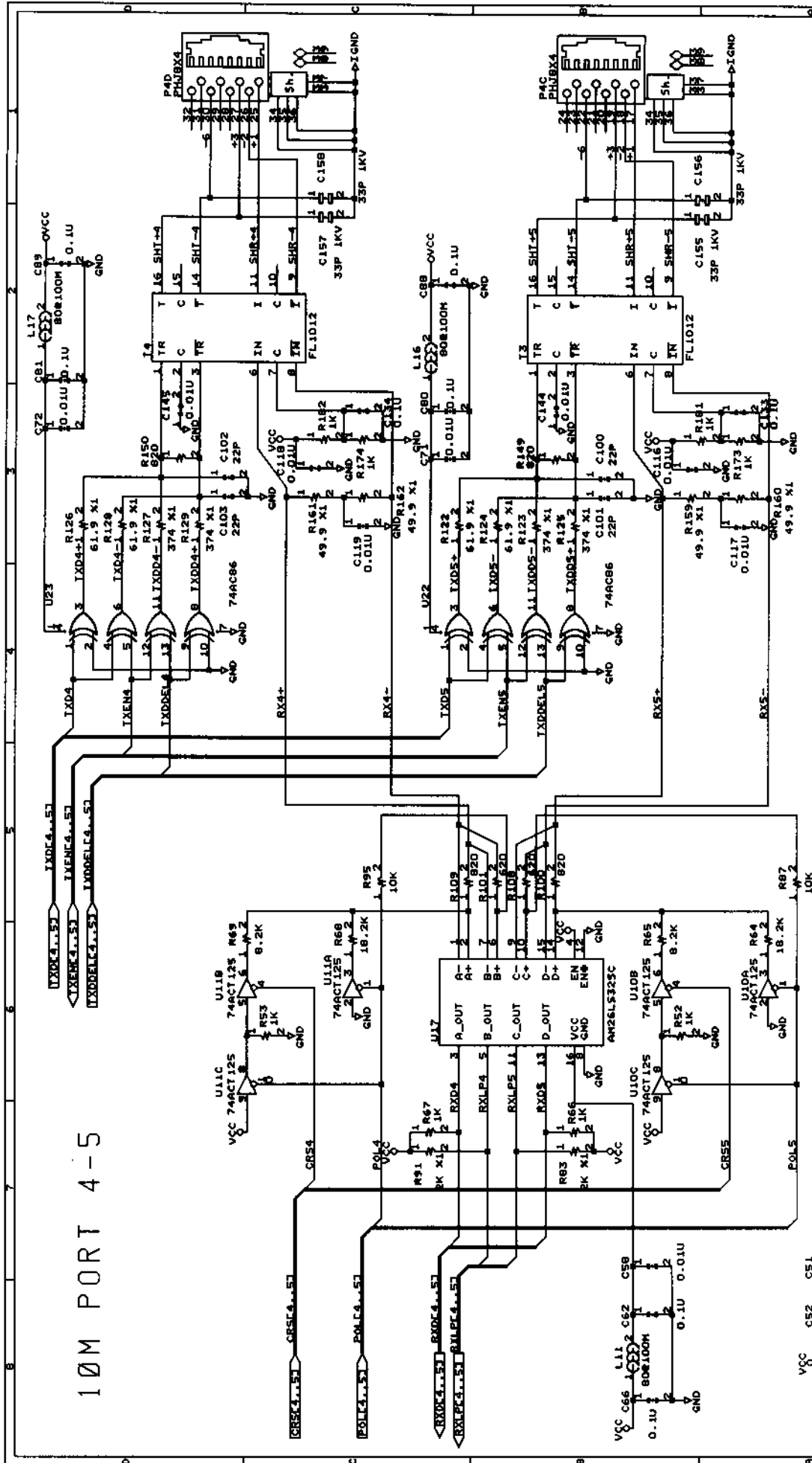
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Date: September 22, 1997 Sheet 9 of 12

10M PORT 4-5



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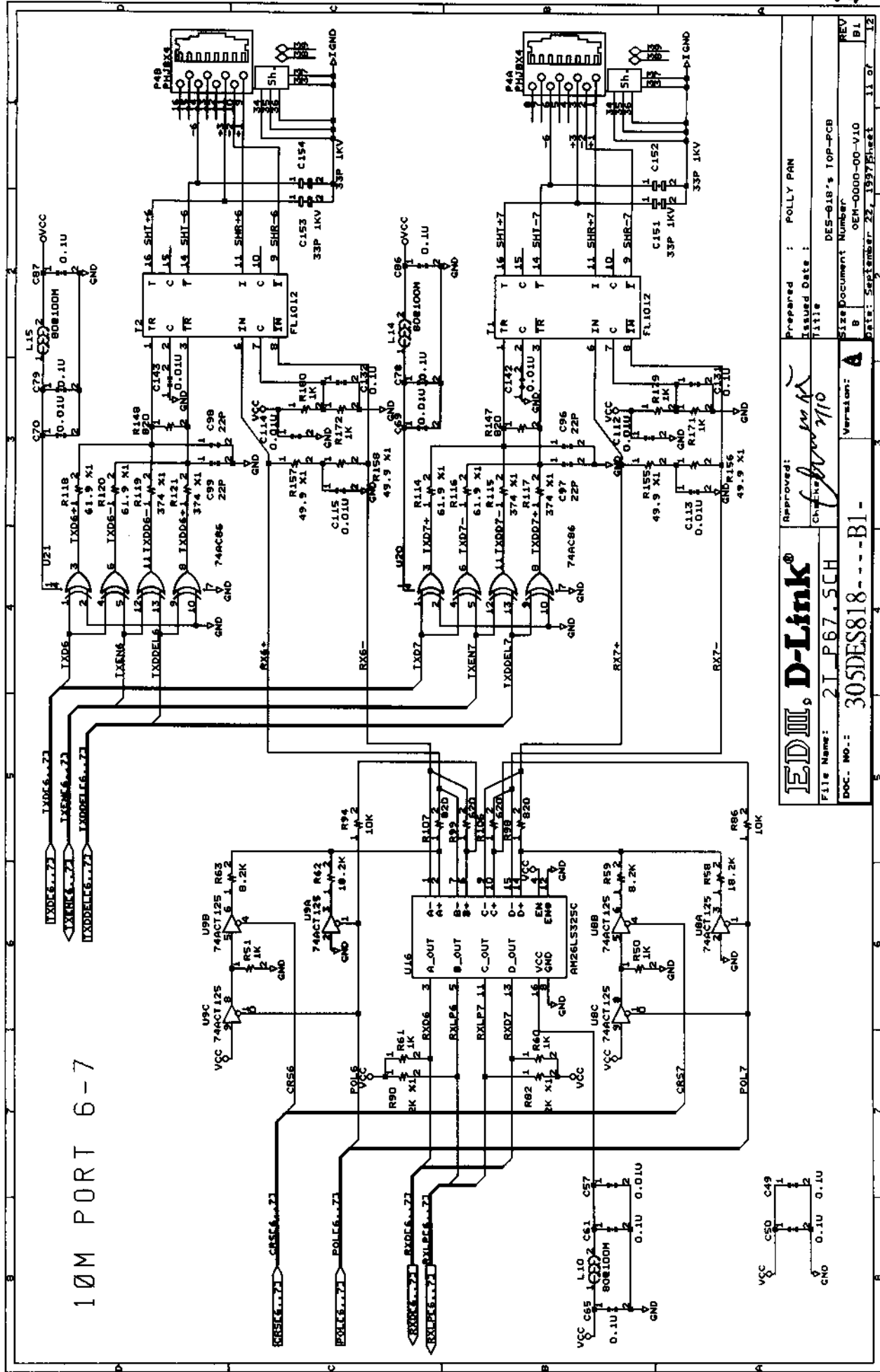
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REV B1 10 of 12

10M PORT 6-7



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DES-018's TOP-PCB

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11 of 12

Date: September 22, 1997

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11 of 12

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11 of 12

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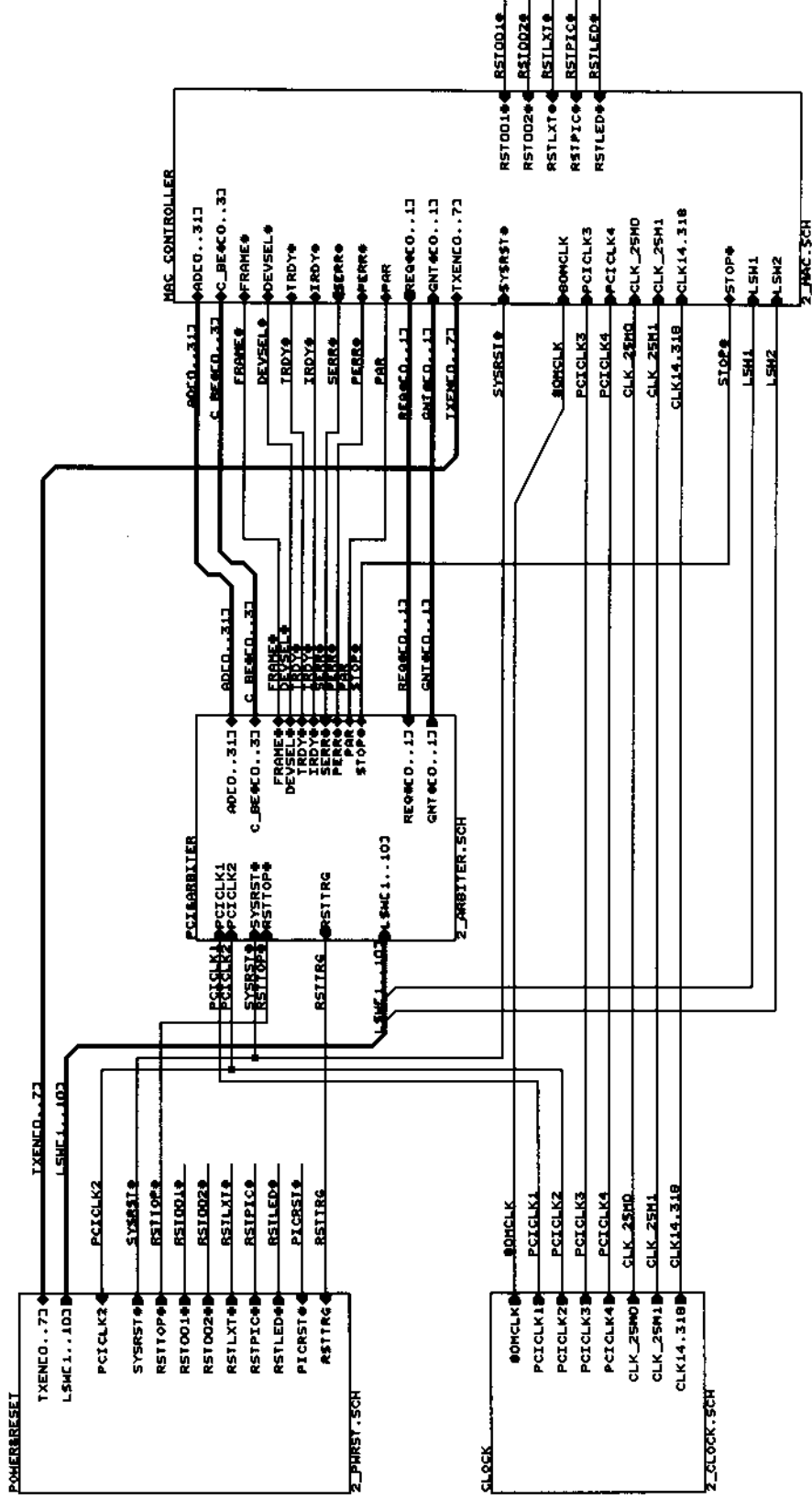
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11 of 12

DES818 LOW-POL Rev.01

DES810 & DES818's LOW_PCB

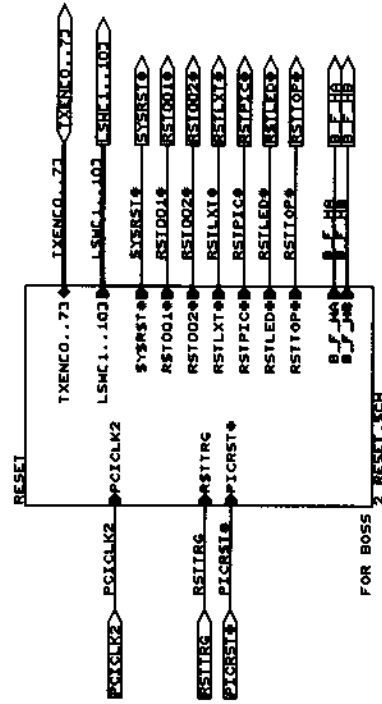
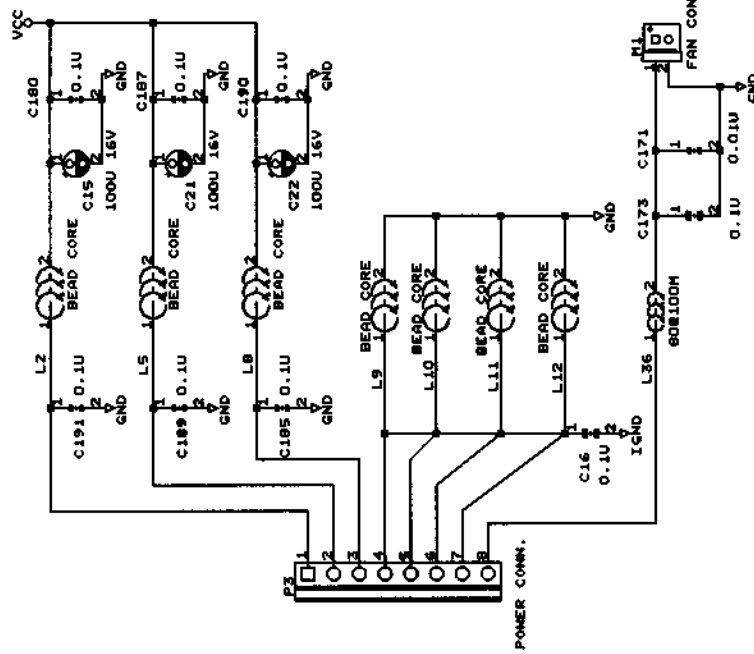


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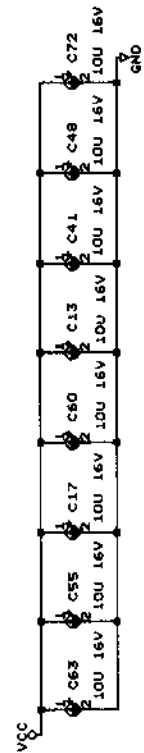
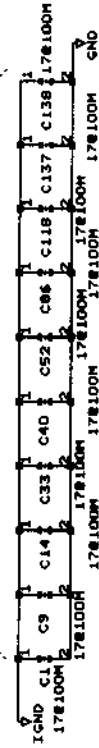
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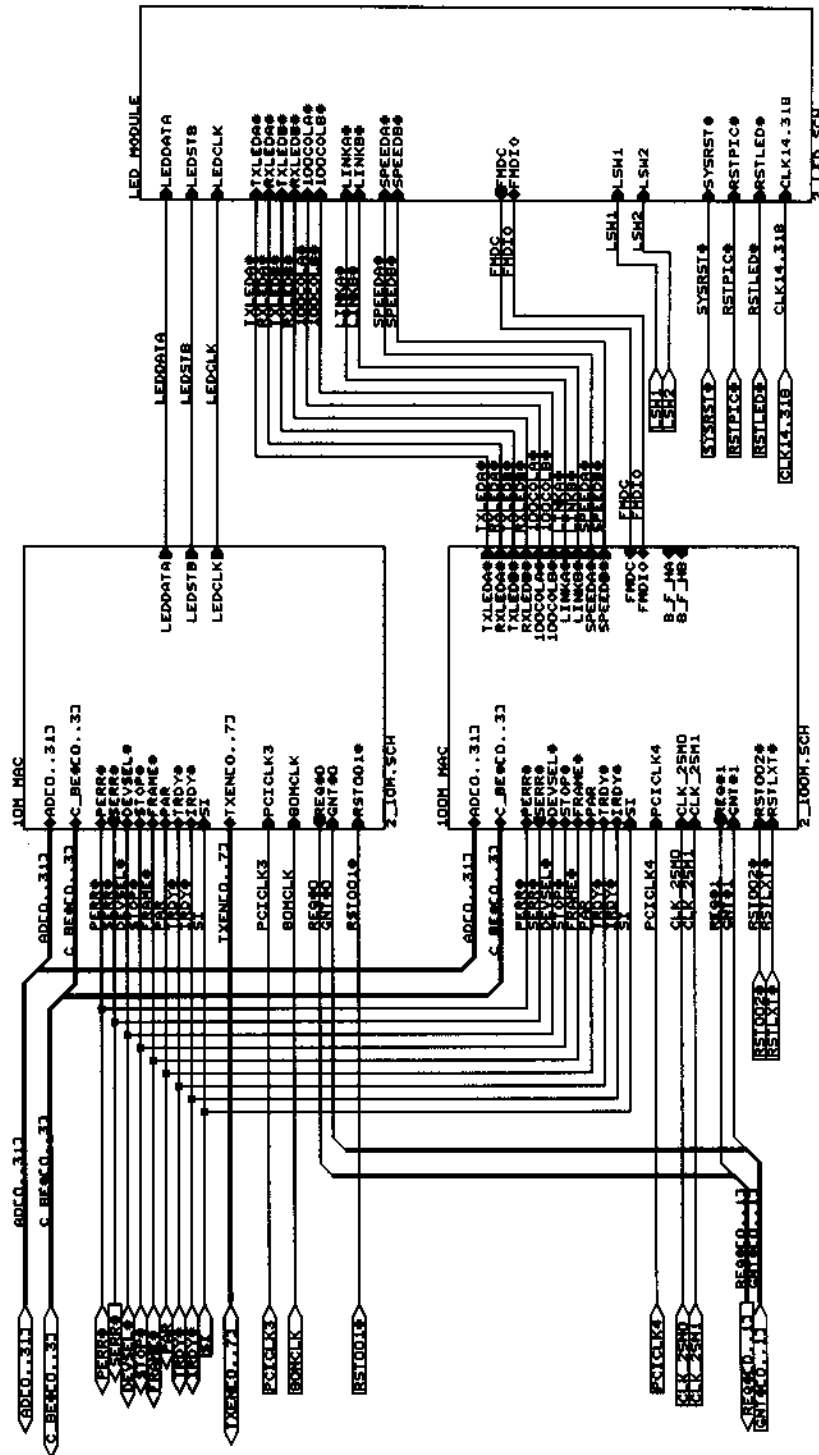
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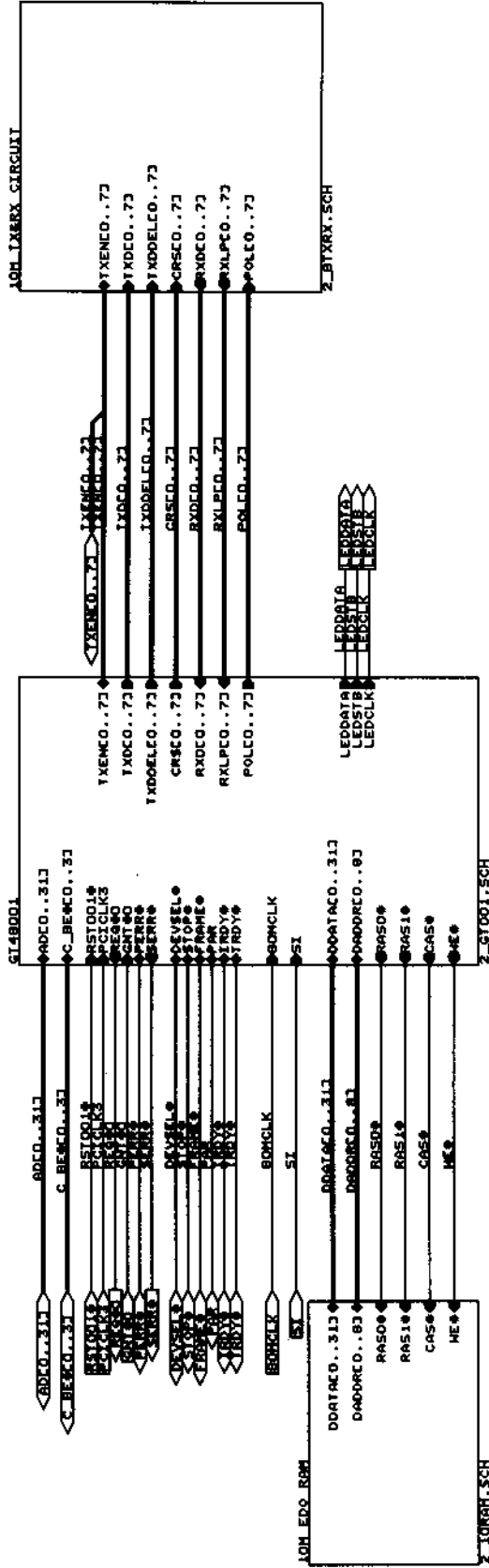
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MAC CONTROLLER



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| | | | Date: October 9, 1997 Sheet 6 of 21 |

10M MAC

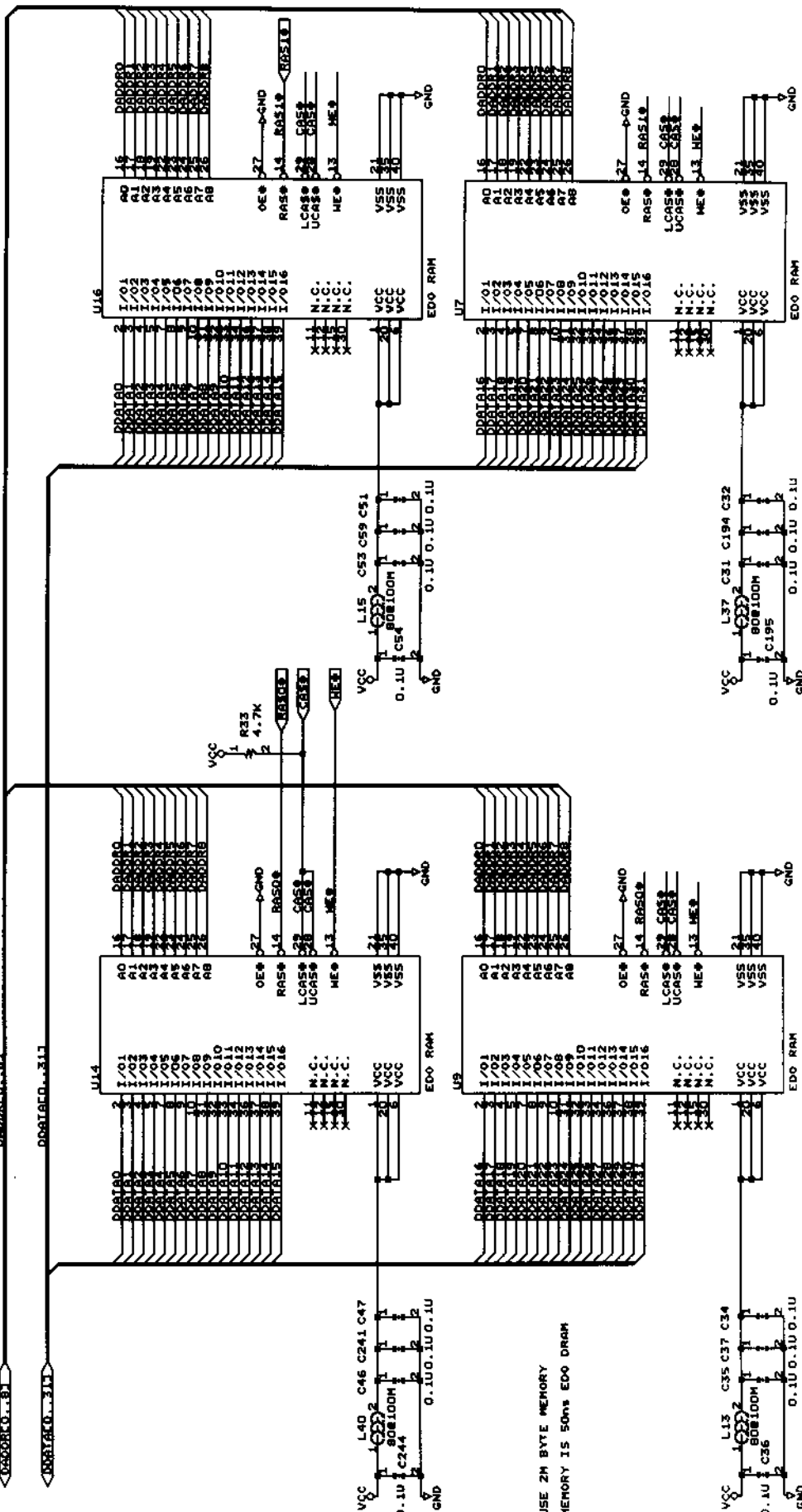


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| DOC. NO.: 305DES818---B1- | | Version: A | Size Document Number: OEN-Q000-00-V10 |
| | | Date: October 9, 1997 | Sheet 7 of 21 |

2MB EDO RAM FOR GT48001A

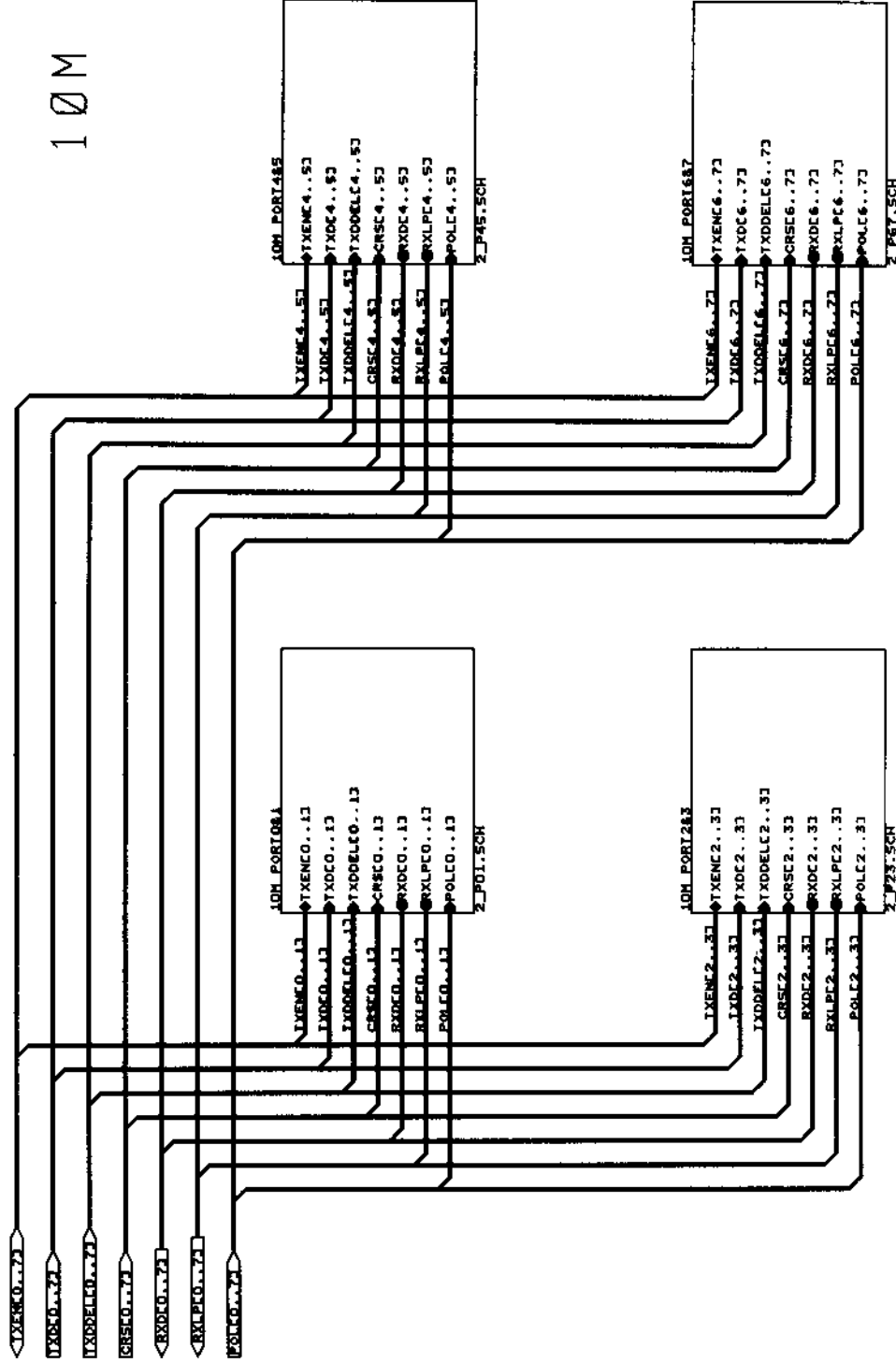
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10M PHY



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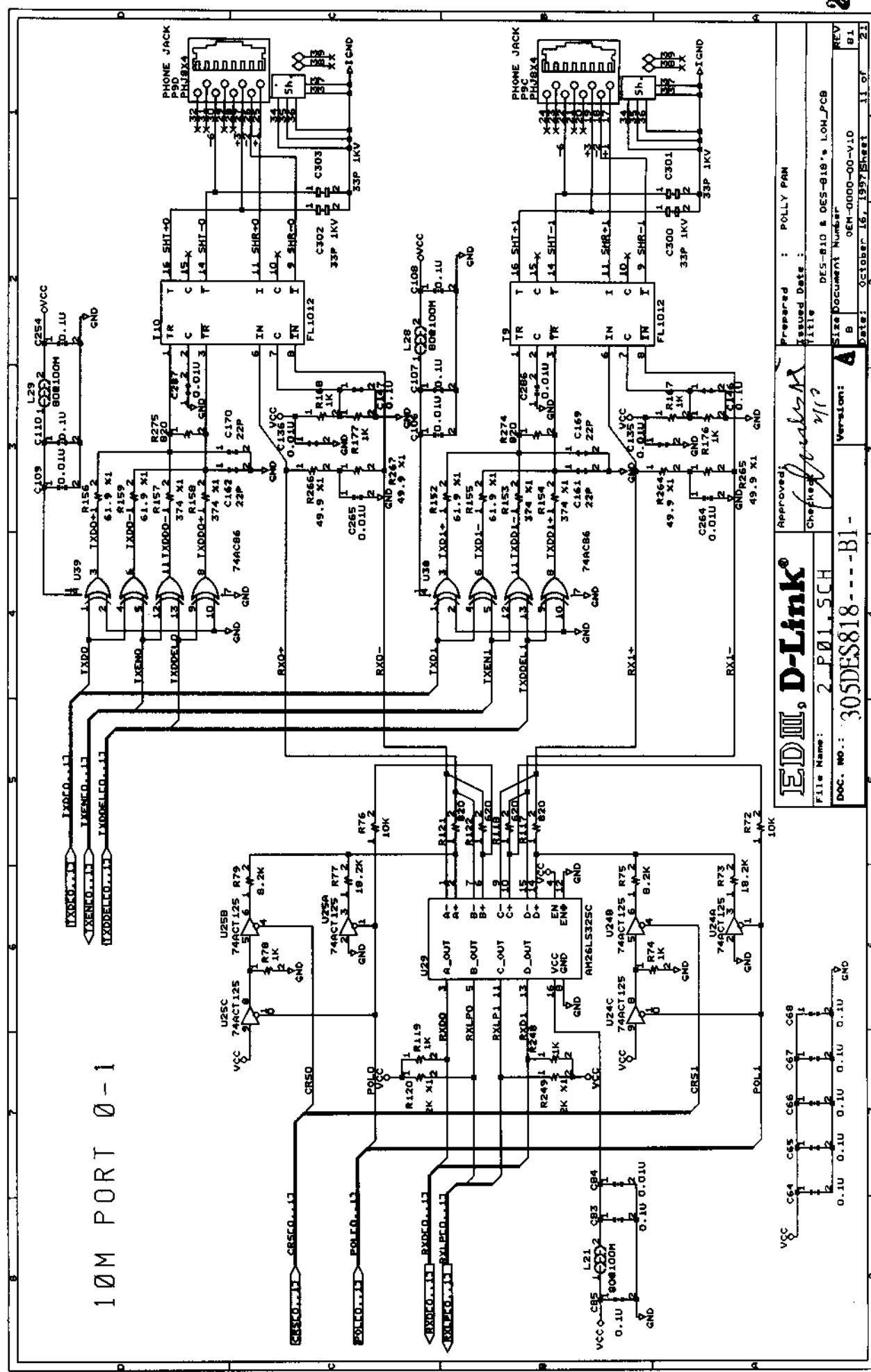
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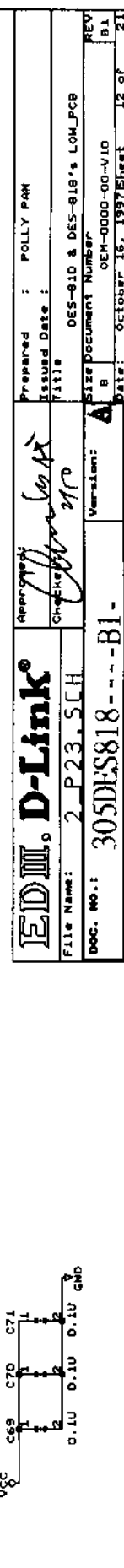
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Doc. No.: 305DES818---B1- Version: A Size Document Number: OEM-0000-00-V10

Date: October 9, 1997 Sheet 10 of 21

22/33





10M PORT 6-7

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DES-81D & DES-81B's LOW PCB

DOC. NO.: 30DES818- - - - B1- REV: 01

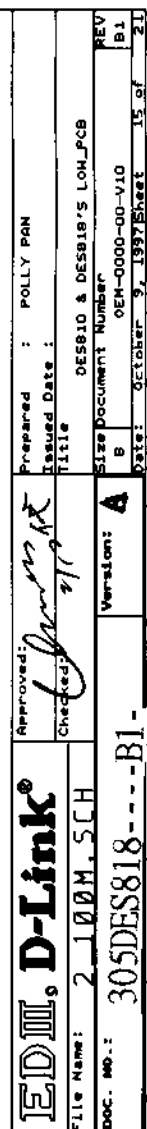
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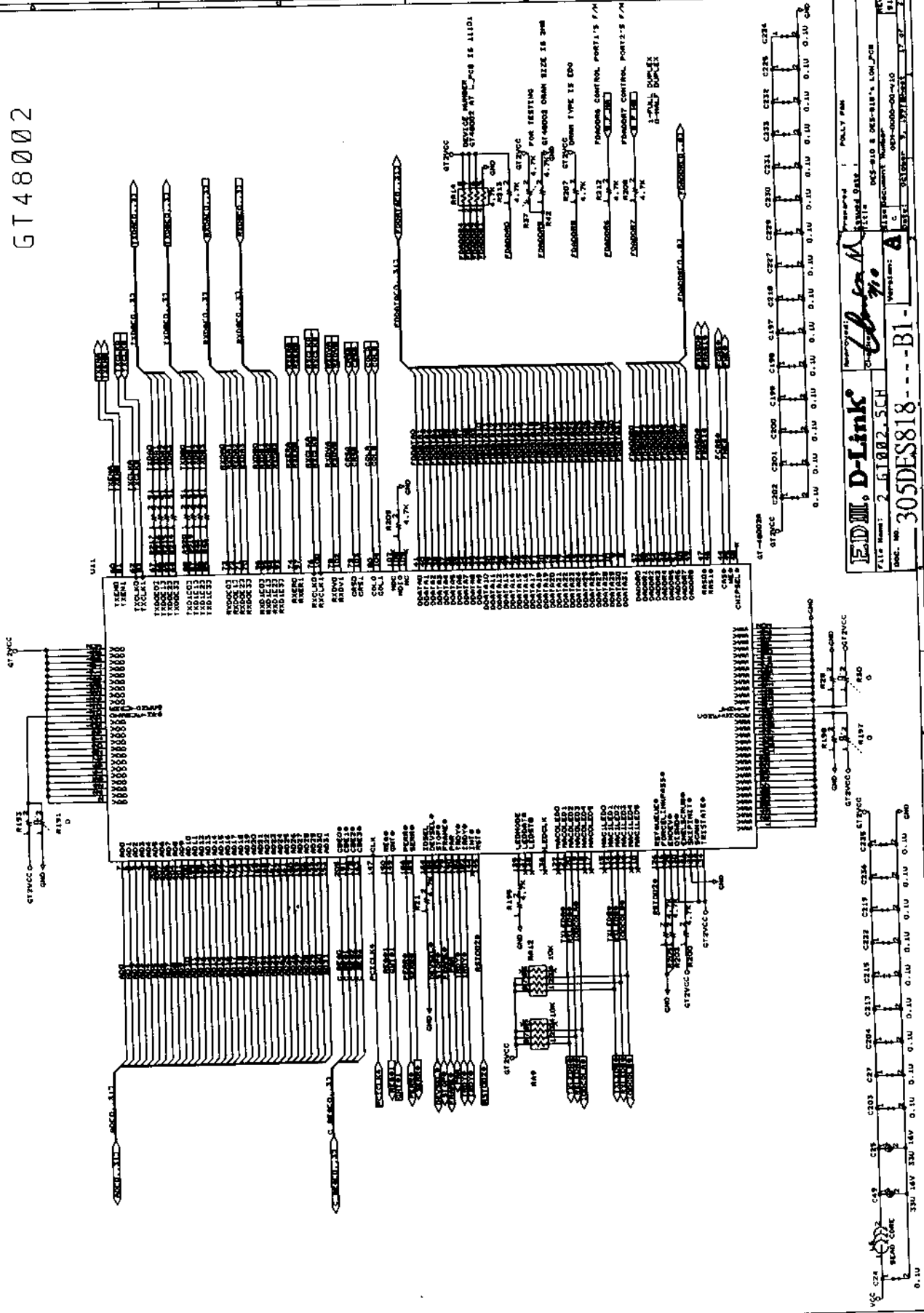
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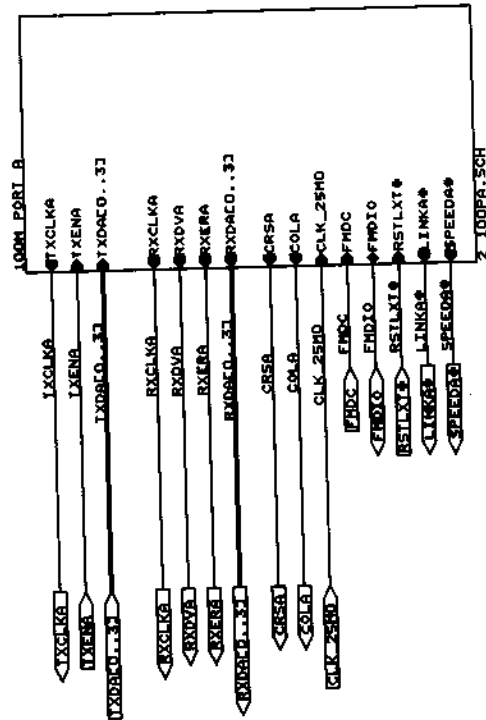
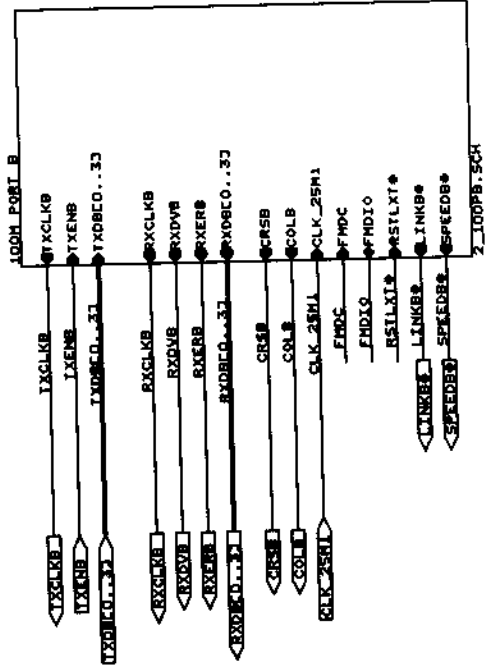
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GT48002



100M PHY



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Date: October 9, 1997 Sheet 18 of 21

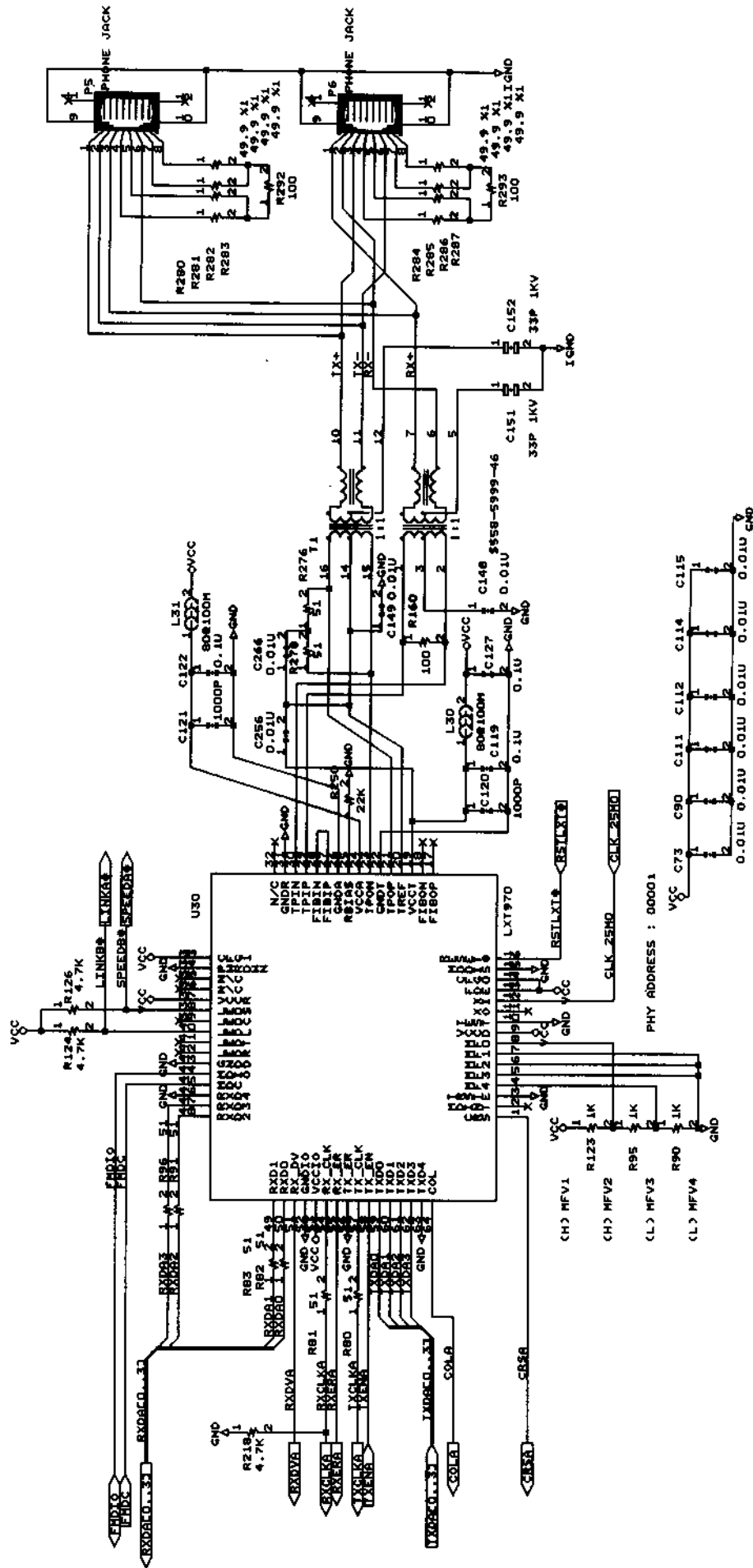
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Doc. No.: 305DES818-...-B1-

Version: A

REV B1

100M PORT1



100M PORT2

PCB Schematic Diagram for 100M PORT2

The diagram shows the internal circuitry of the 100M PORT2 module, including the connector pinout, internal components, and the connection to the host system.

Connector Pinout:

- 1: VCC
- 2: 4.7K
- 3: 4.7K
- 4: 4.7K
- 5: 4.7K
- 6: 4.7K
- 7: 4.7K
- 8: 4.7K
- 9: 4.7K
- 10: 4.7K
- 11: 4.7K
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- 91: 4.7K
- 92: 4.7K
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- 95: 4.7K
- 96: 4.7K
- 97: 4.7K
- 98: 4.7K
- 99: 4.7K
- 100: 4.7K

Internal Components:

- U31: 100M PORT2 IC
- R125: 4.7K
- R126: 4.7K
- R127: 4.7K
- R128: 4.7K
- R129: 4.7K
- R130: 4.7K
- R131: 4.7K
- R132: 4.7K
- R133: 4.7K
- R134: 4.7K
- R135: 4.7K
- R136: 4.7K
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Prepared : POLLY PAN

Issue Date :

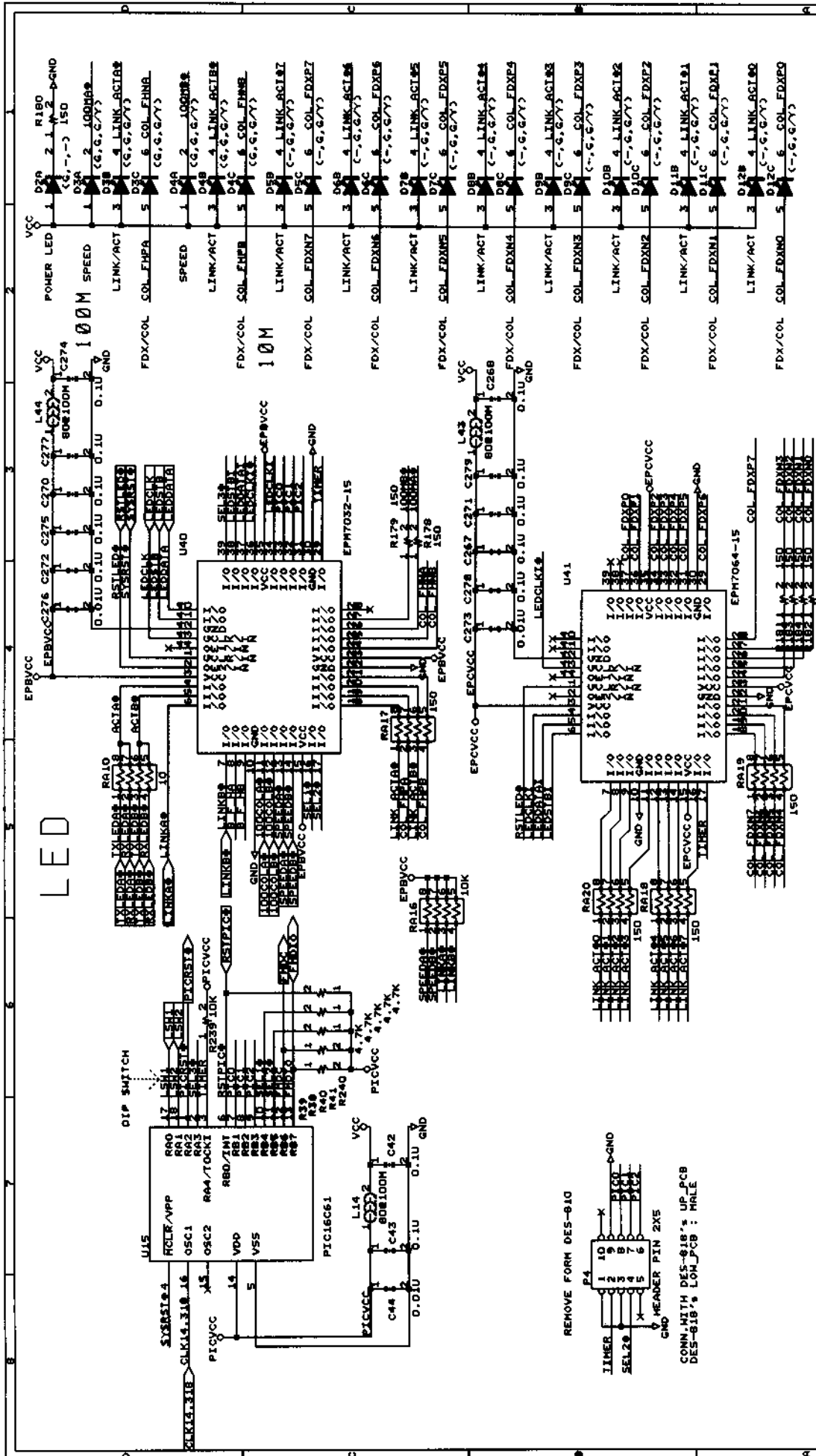
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