



# GRILL

DES 818 Rev. A1

生效日期: 87. 3. 17

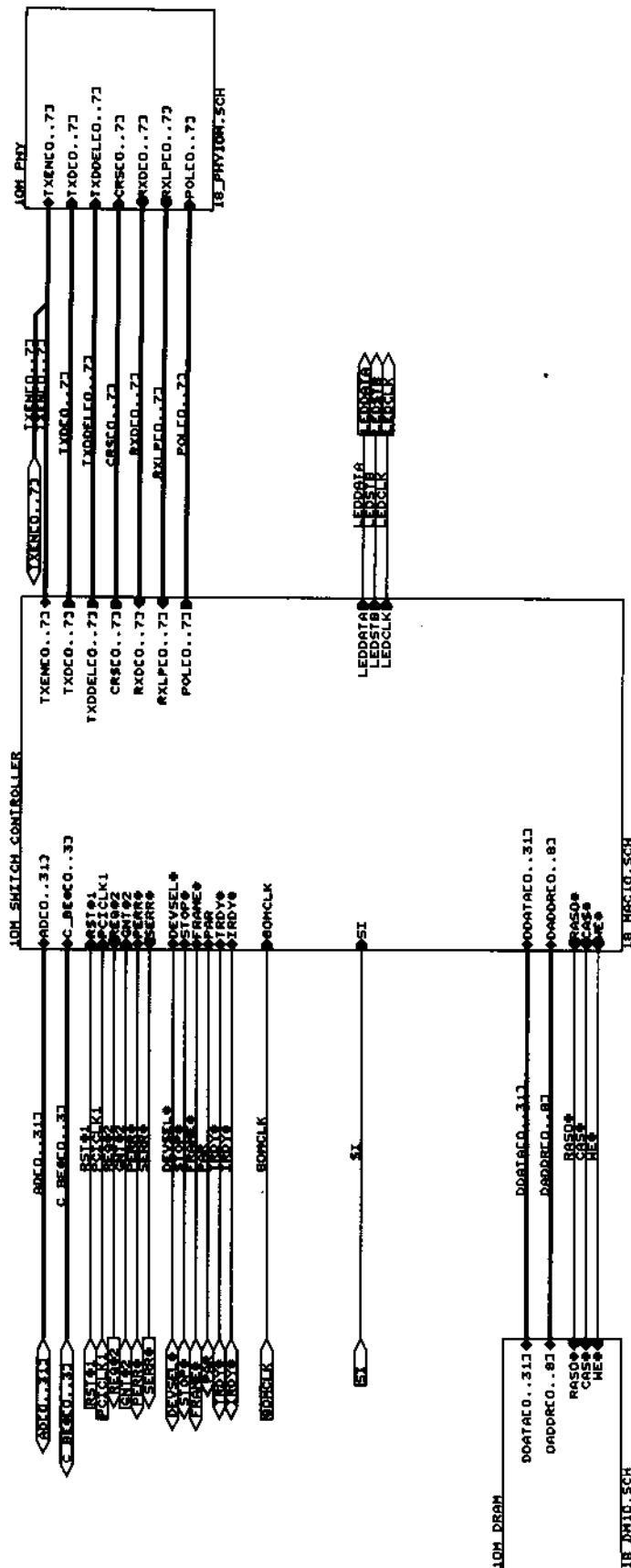
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APPROVED	CHECKED		DEPARTMENT	PREPARED
李福是校	X	X	2023	Polly 29



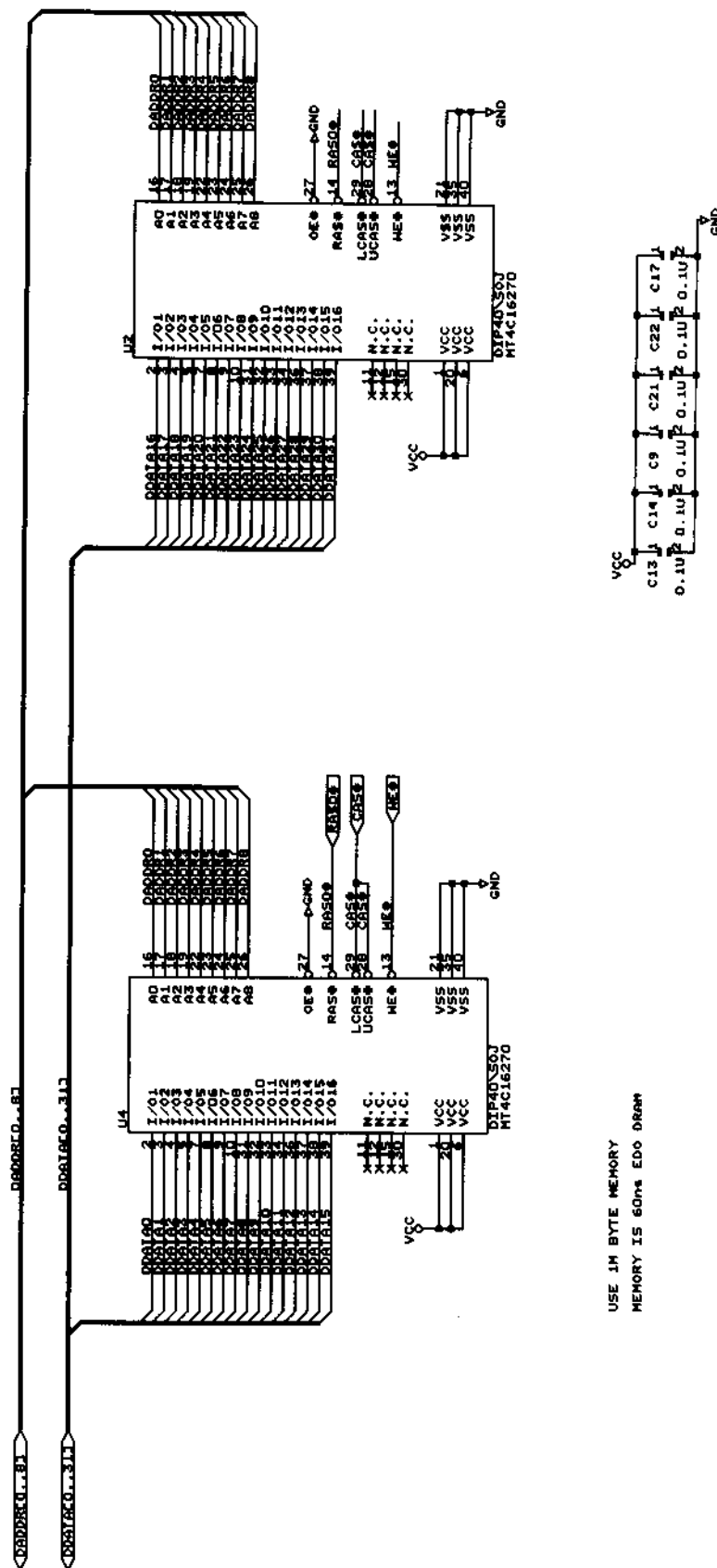


# 10M MAC CONTROLLER



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DOC. NO.: 305DES18-...-A1-		Checked: <i>[Signature]</i>	Issued Date:
Version: A		Size Document Number: 8	DES-018's UP PCB
Date: March 10, 1997		Sheet 2 of 12	REV A1

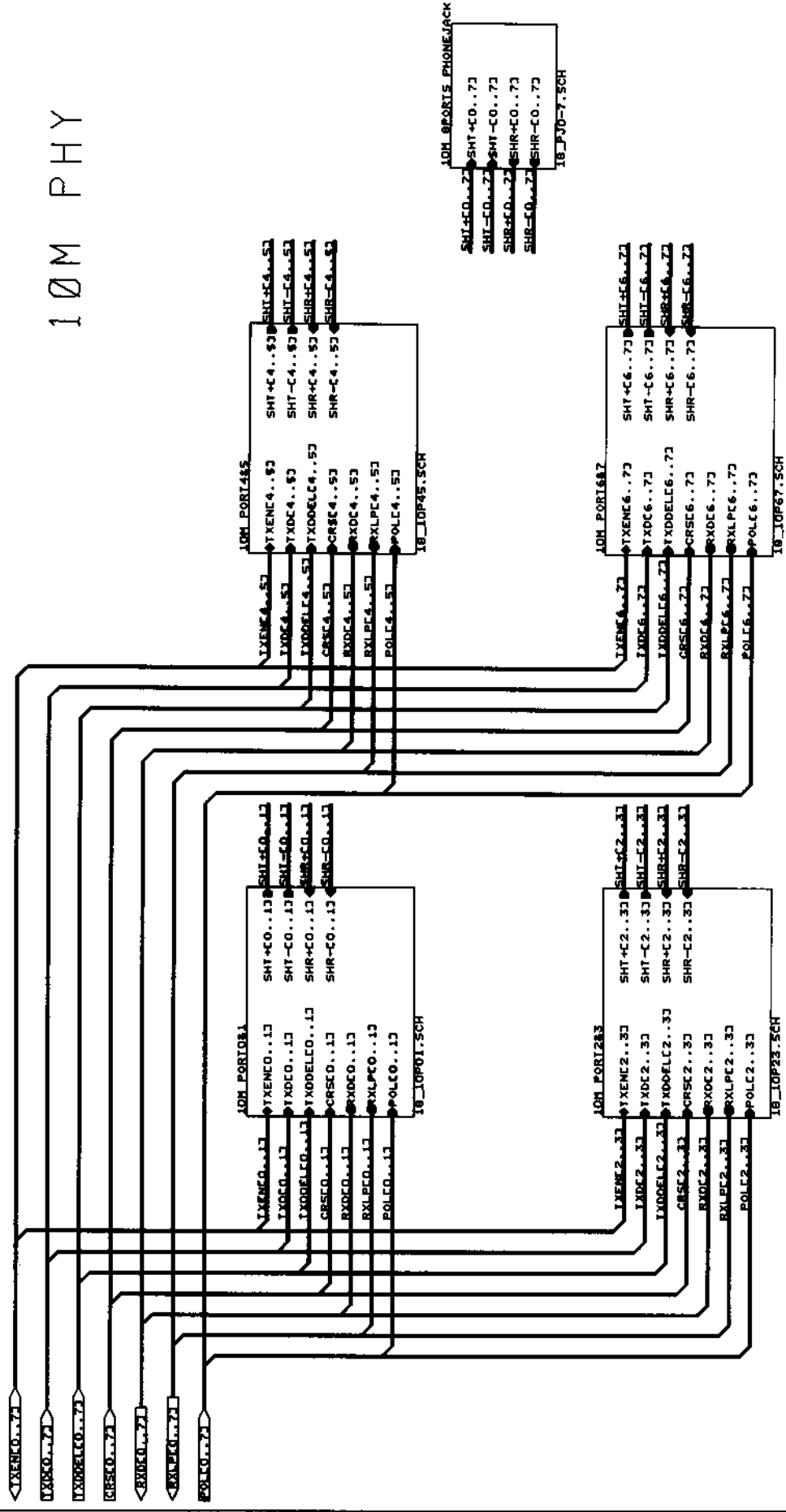
DRAM FOR GT48001



USE 1M BYTE MEMORY  
MEMORY IS 60ms EDO DRAM

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DOC. NO.: 305DES18- - - -A1 -		Version: <b>A</b>	DES-818's UP_PCB
		Size Document Number	
		B	OE#-0000-00-V1.0
		Date: 5 March 10, 1997	Sheet 3 of 12

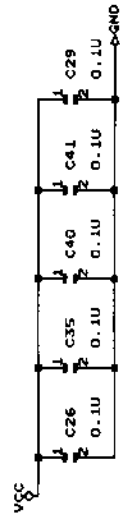
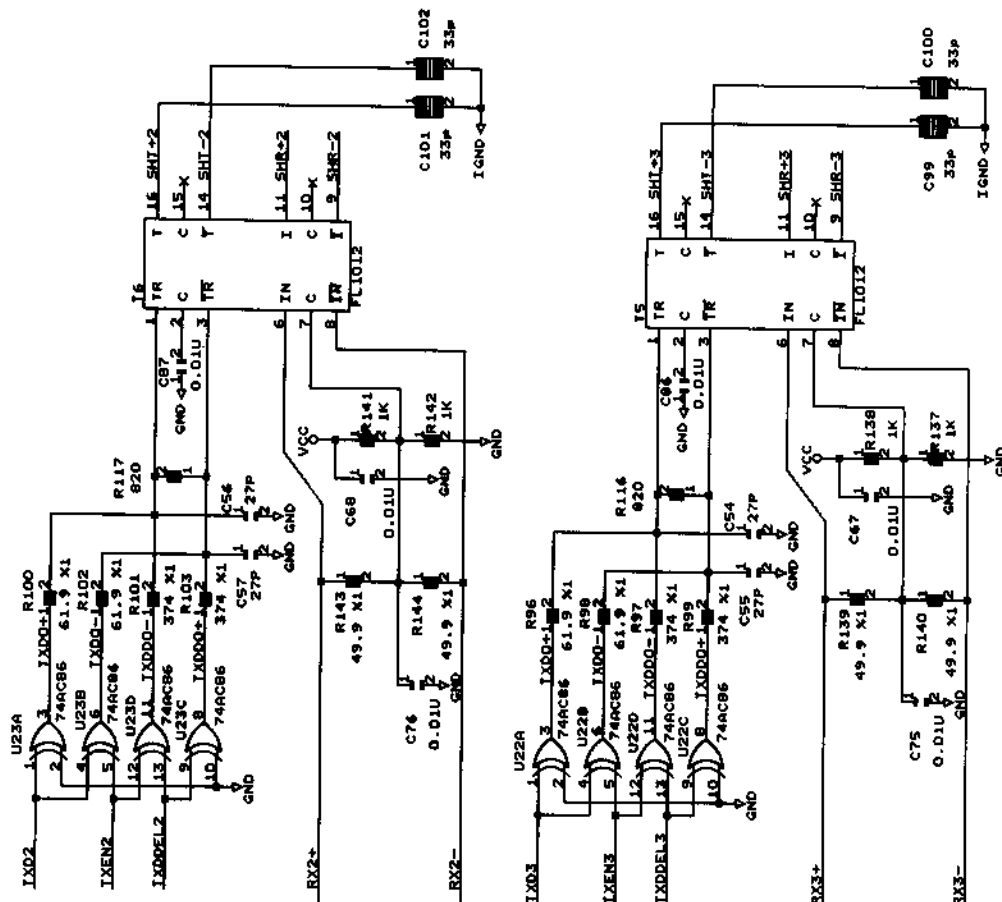
# 10M PHY



10M\_PORTS\_PHONEJACK  
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DOC. NO.: 305DES818- --A1-		Version: A		Issued Date:	
Size Document Number		DES-818's UP_PCB		REV	
OEM-0000-00-V10		Date: March 10, 1997		AL	
Sheet 4 of 12					





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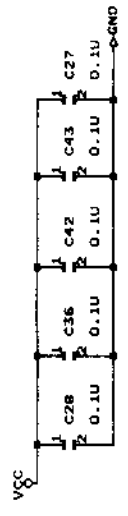
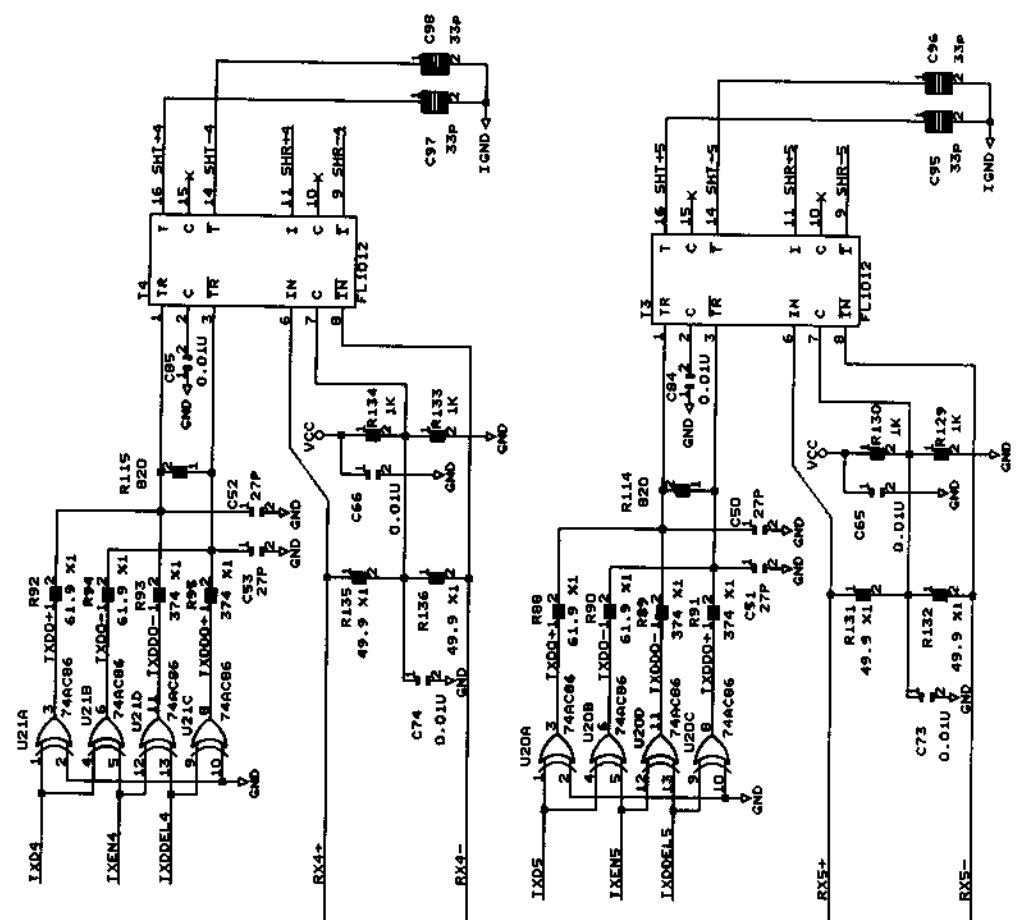
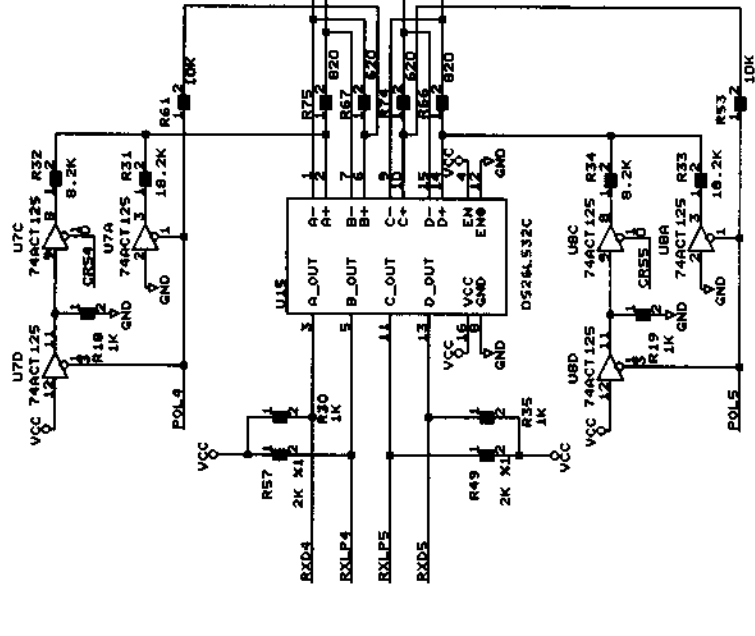
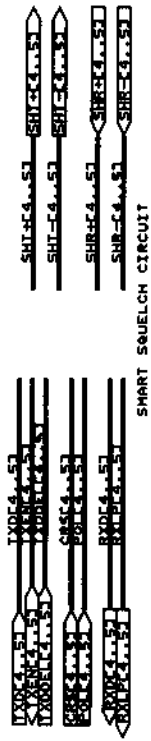
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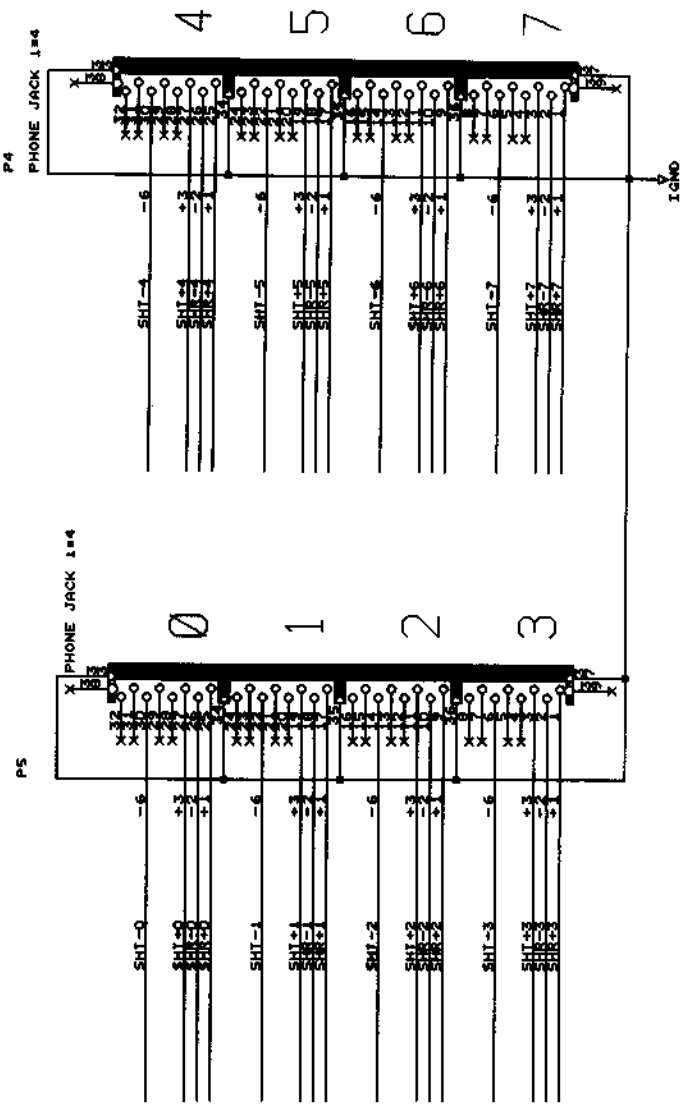


# 10M PHY PORT4-5



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Doc. No.: 305DES18-1-A1		Issued Date :
Version: 1		Size Document Number
Date: 12/12/1997		Page 1 of 12

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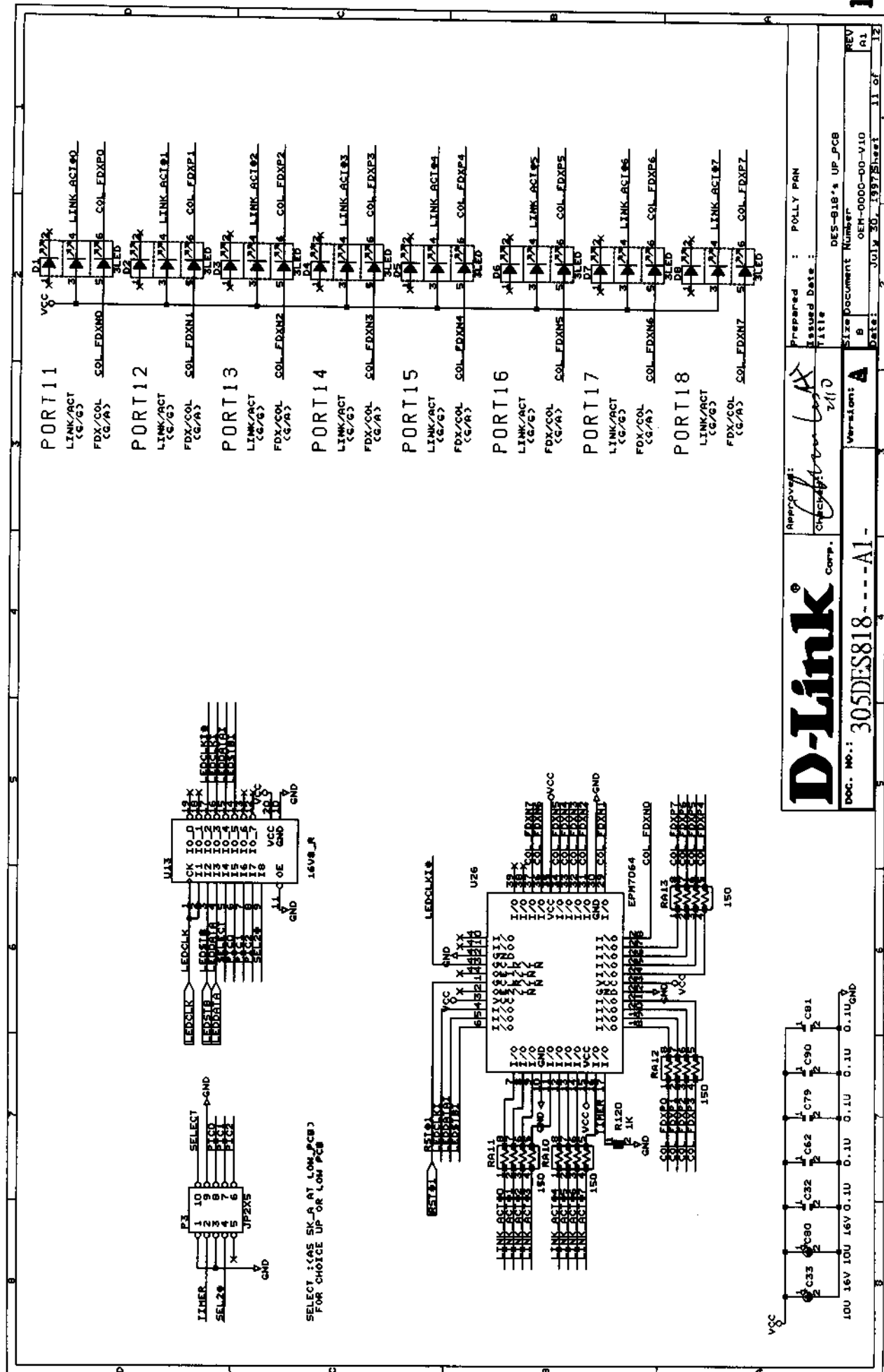
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DOC. NO.: 305DES818---A1-

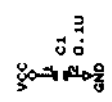
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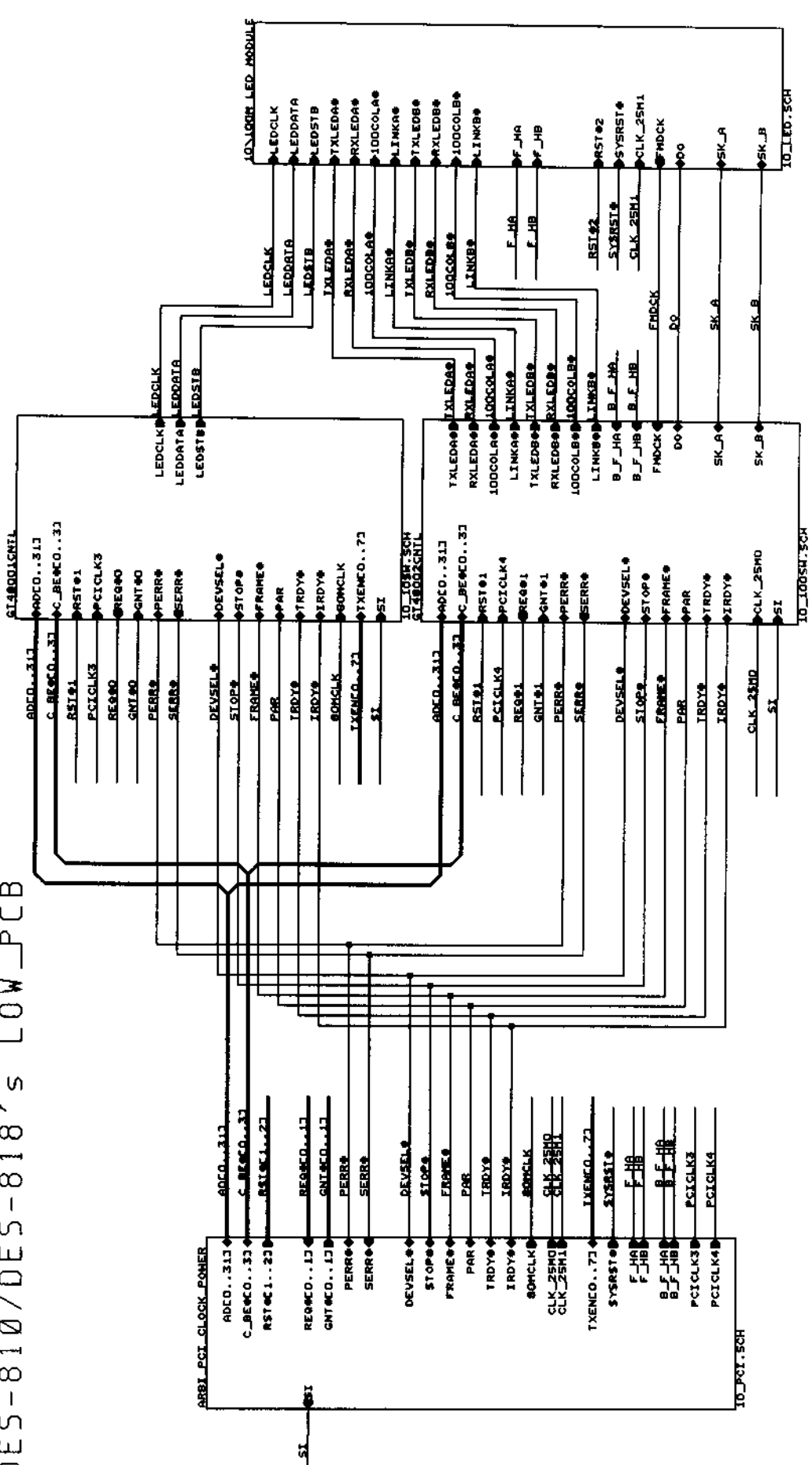


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DOC. NO.: 305DES818-...A1-

Size	Document Number	REV
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Date:	March 5, 1997	Sheet of 21

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DES-010-18, LOWCB

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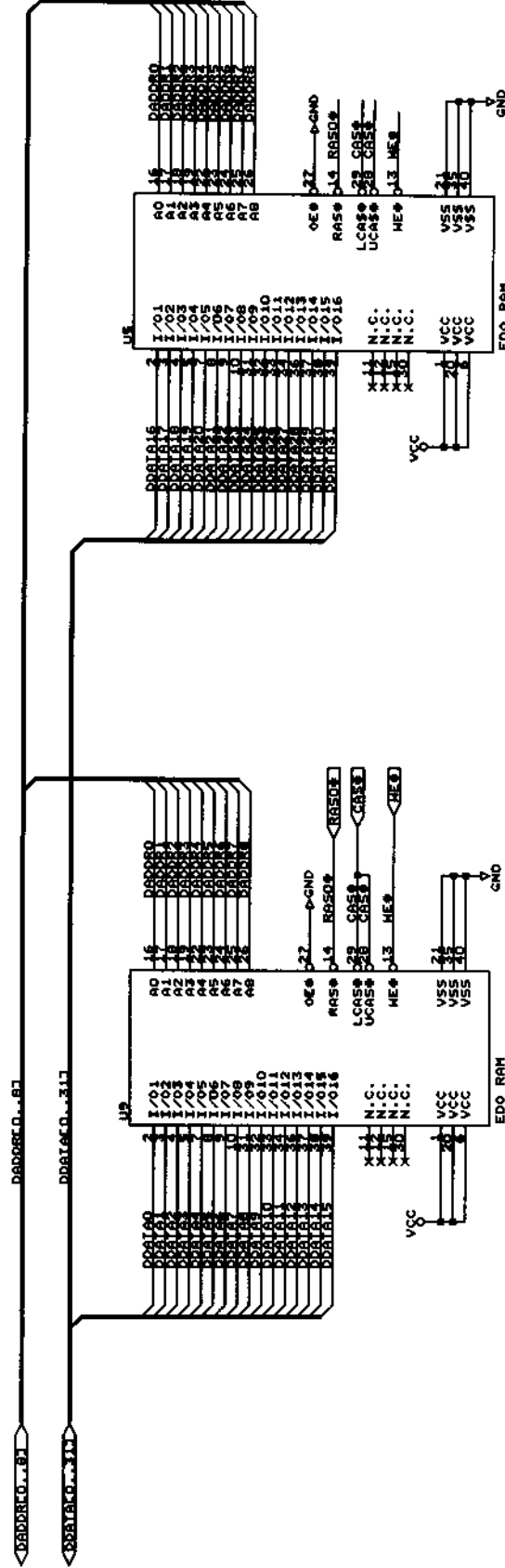
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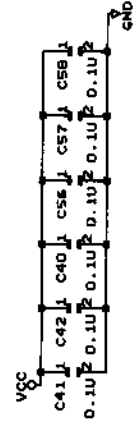
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# DRAM FOR GT48001



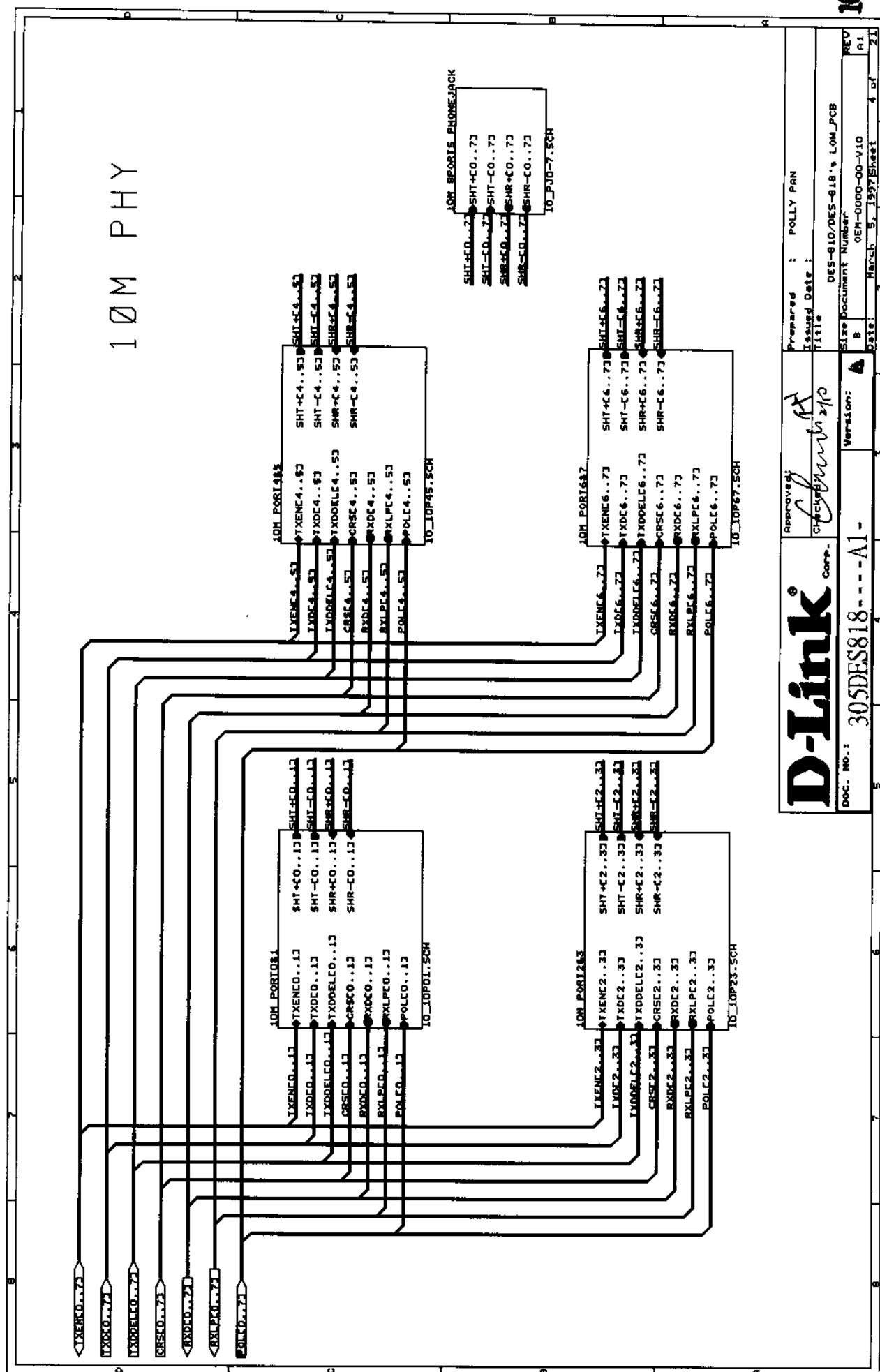
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MEMORY IS 60ns EDO DRAM

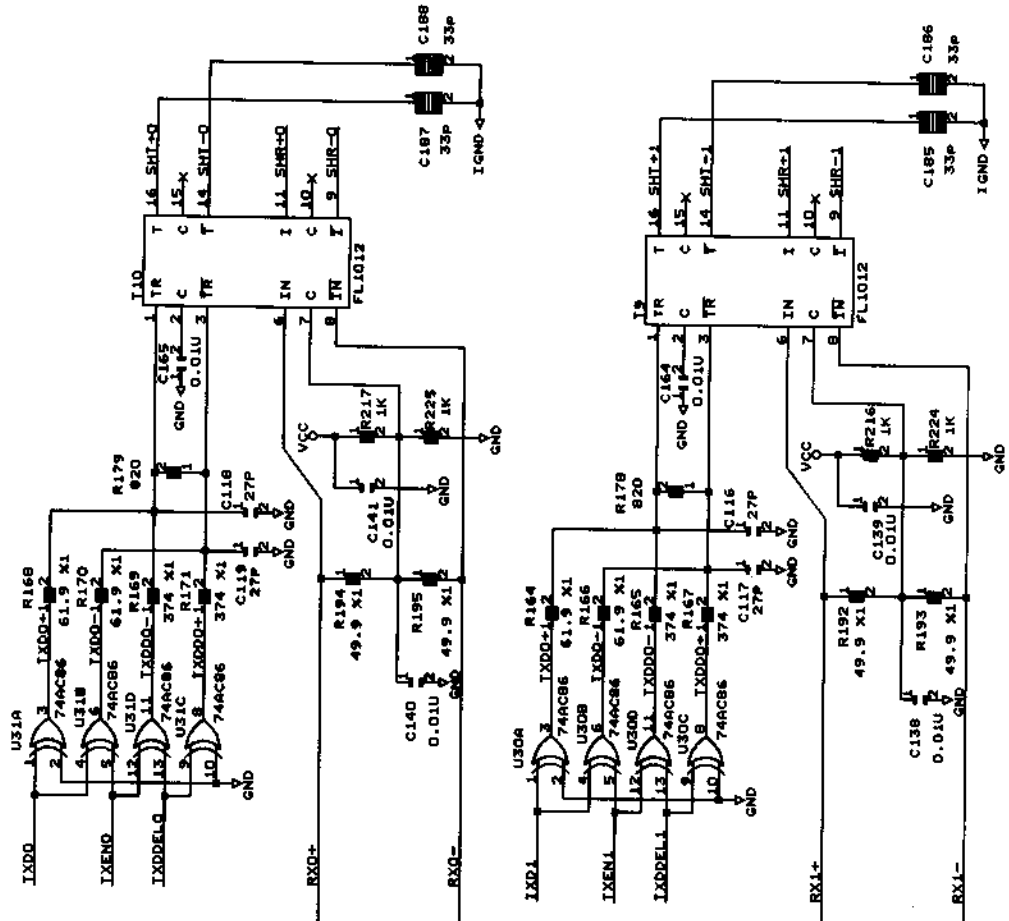
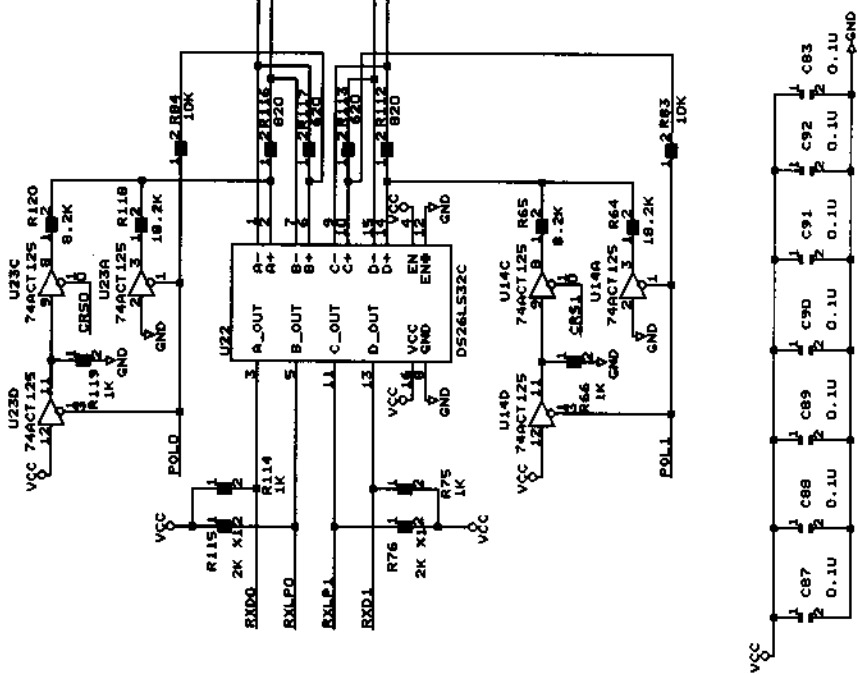


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Title: DES-810/DES-818's LON\_PCB

DOC. NO.: 305DES818--A1-	Version: A	Size Document Number: B	REV: A1
Date: March 19, 1997	Page: 3 of 31		



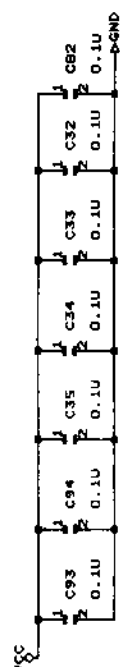
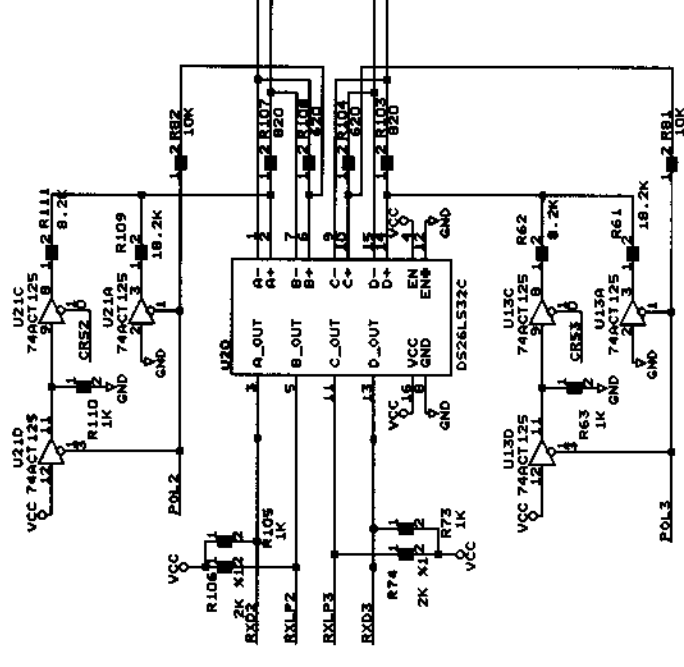


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DOC. NO.: 305DES818-A1-

Prepared : POLLY PAN  
 Issued Date :  
 File  
 DES-010/DES-018  
 Size Document Number  
 8  
 Date: June 10, 1997

Figure 1: Schematic representation of the 12S rRNA gene organization. The diagram shows the 12S rRNA gene (16S) and the 16S rRNA gene (16S) with their respective introns and exons. The 12S rRNA gene is shown as a single line with introns indicated by arrows. The 16S rRNA gene is shown as a double line with introns indicated by arrows. The 12S rRNA gene is transcribed into 12S rRNA, which is then processed into 12S rRNA. The 16S rRNA gene is transcribed into 16S rRNA, which is then processed into 16S rRNA. The 12S rRNA and 16S rRNA are then assembled into the 12S and 16S ribosomal subunits, respectively.

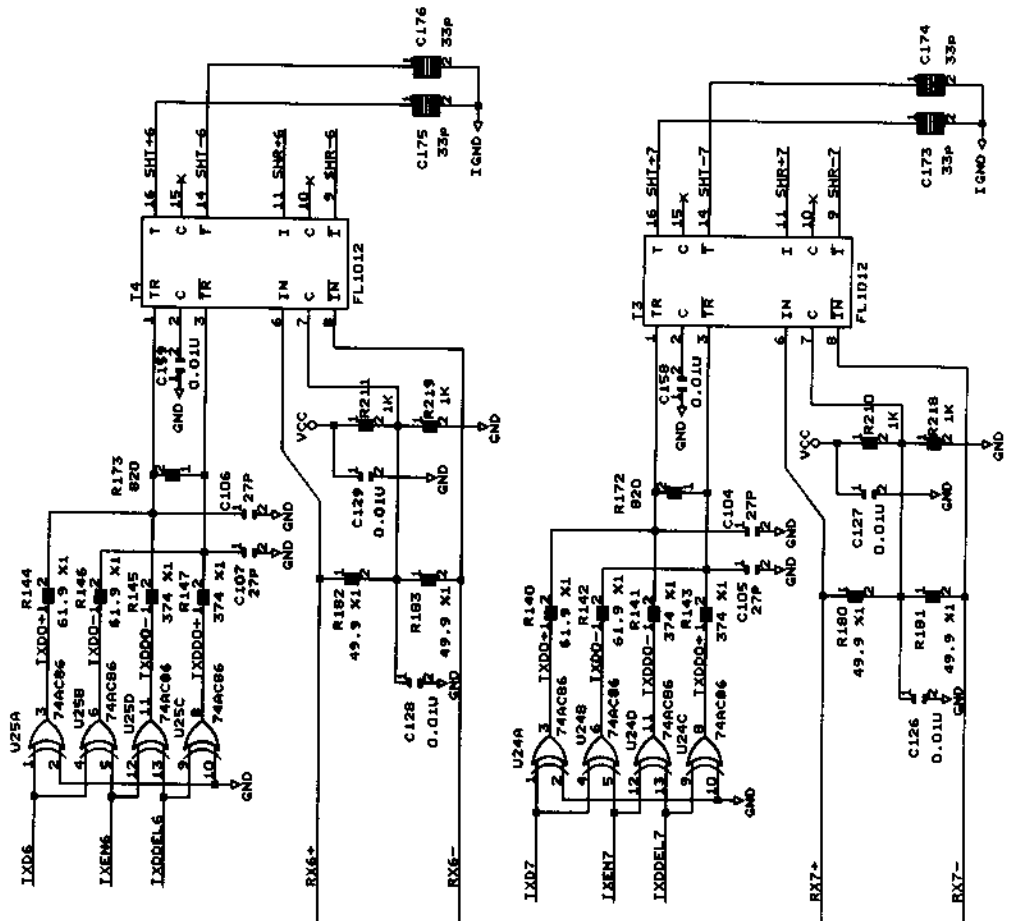
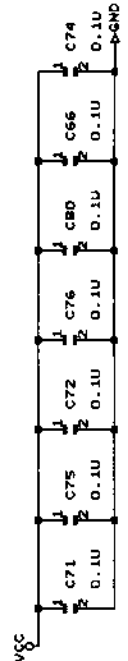
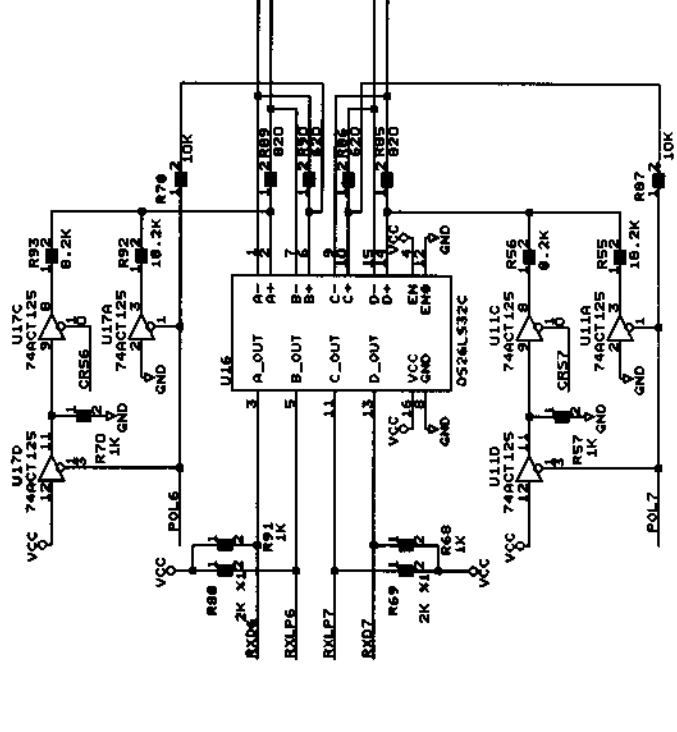


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# 10M PHY PORT6-7



**D-Link** Corp.

DOC. NO.: 305DES18---A1-

Approved: *Charles Sio*

Checked: *Charles Sio*

Prepared: POLLY PAN

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Title: DES-810/DES-818's LON\_PCB

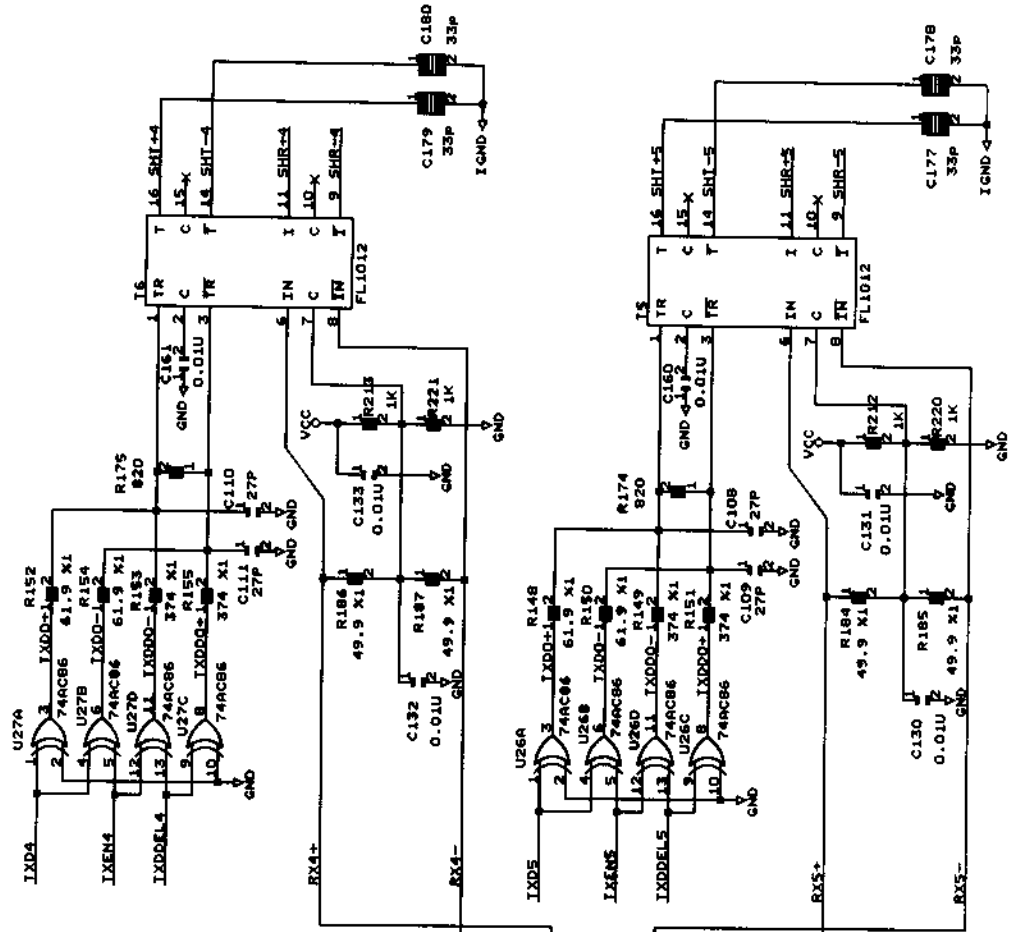
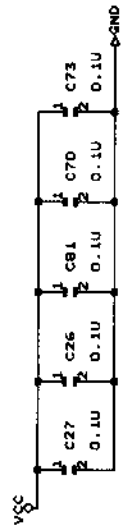
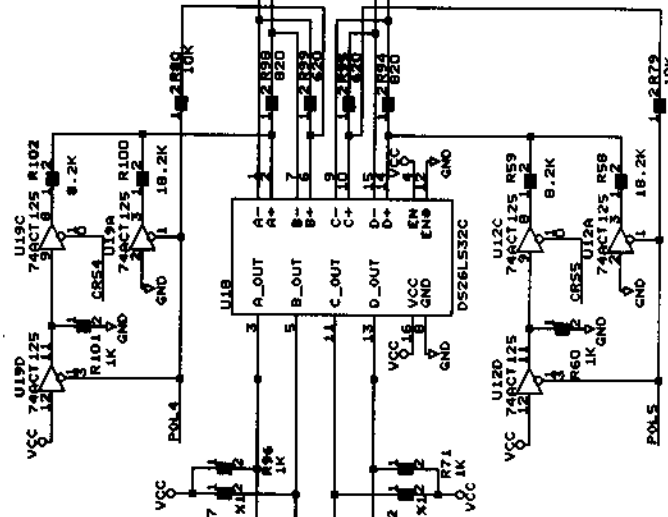
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Date: May 12, 1997

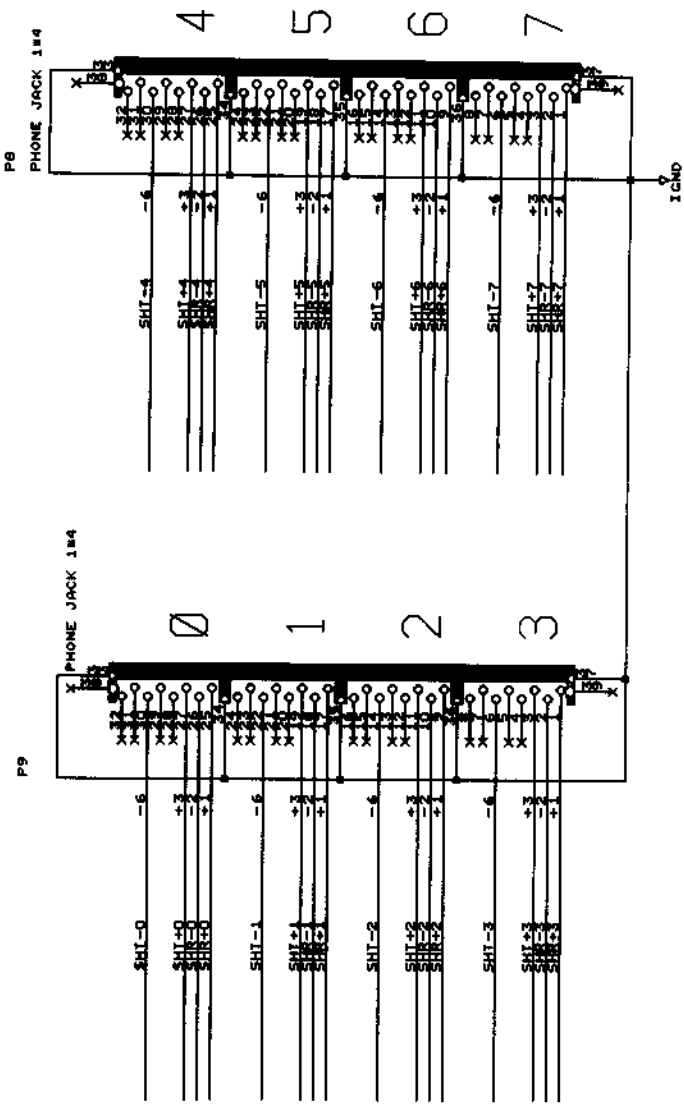
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# 10M PHY PORT4-5



<b>D-Link</b> Corp.		Approved: <i>[Signature]</i> Checked: <i>[Signature]</i>	Prepared: POLLY PAN Issued Date:
DOC. NO.: 305DES818---A1-		Version: A	DES-810/DES-818's LOM_PCB Size Document Number: 8 Date: Nov 12, 1997
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<b>D-Link</b> Comp.	Approved: <i>[Signature]</i>	Prepared: POLLY PAN
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	Version: A	DES-810/DES-818's LOW PCB
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SERIAL MODE PER PORT

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## DD-Link

Sec. no 305DES18 ---A1-  
Version: A  
File Document Number 2  
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The diagram illustrates the 100M MAC CONTROLLER, showing its internal components and external connections. The central block is the 100M SWITCH CONTROLLER, which interfaces with the 100M PHY (top) and the 100M DMA (bottom).

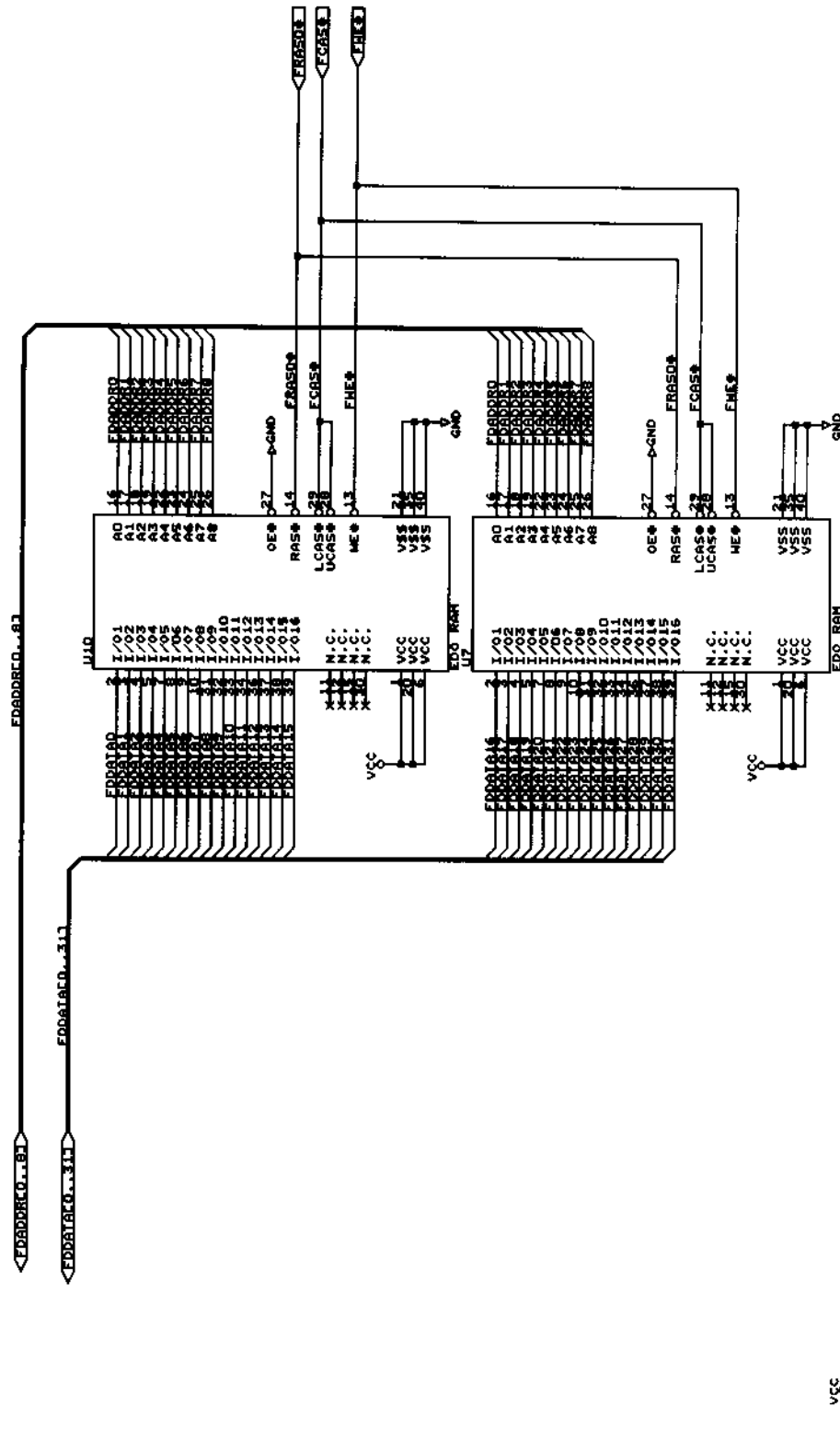
**100M PHY Connections:**

- TXENCB..93, TXCLKB..93, TXDBCB..93, TXD9CB..93, RXDBCB..93, RXD9CB..93, RXENCB..93, RXCLKB..93, RXDVCB..93, CRSCB..93, COLCB..93, CLK\_25M0, CLK\_25M0
- LINKA0, LINKB0, FMDCK, D0, SK\_A, SK\_B

**100M SWITCH CONTROLLER Connections:**

- TXENCB..93, TXCLKB..93, TXDBCB..93, TXD9CB..93, RXDBCB..93, RXD9CB..93, RXENCB..93, RXCLKB..93, RXDVCB..93, CRSCB..93, COLCB..93, CLK\_25M0, CLK\_25M0
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# DRAM FOR GT48002 IS 1MB



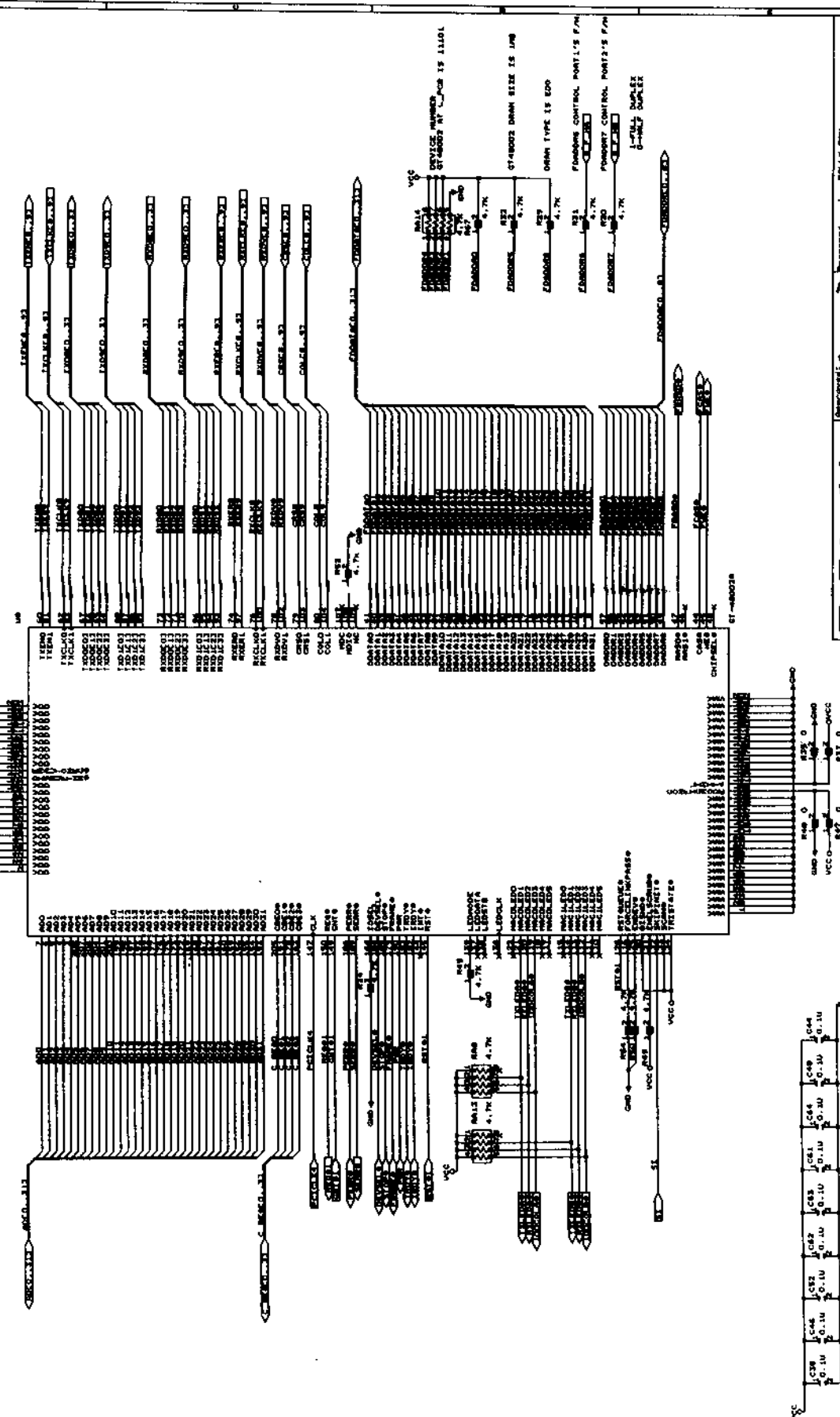
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Prepared: POLLY PAN  
Issued Date:   
Title: DES-810/DES-818's LON\_PCB

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Version:	A	
Size Document Number:	B	
Date:	MARCH 19, 1997	Page 1 of 21

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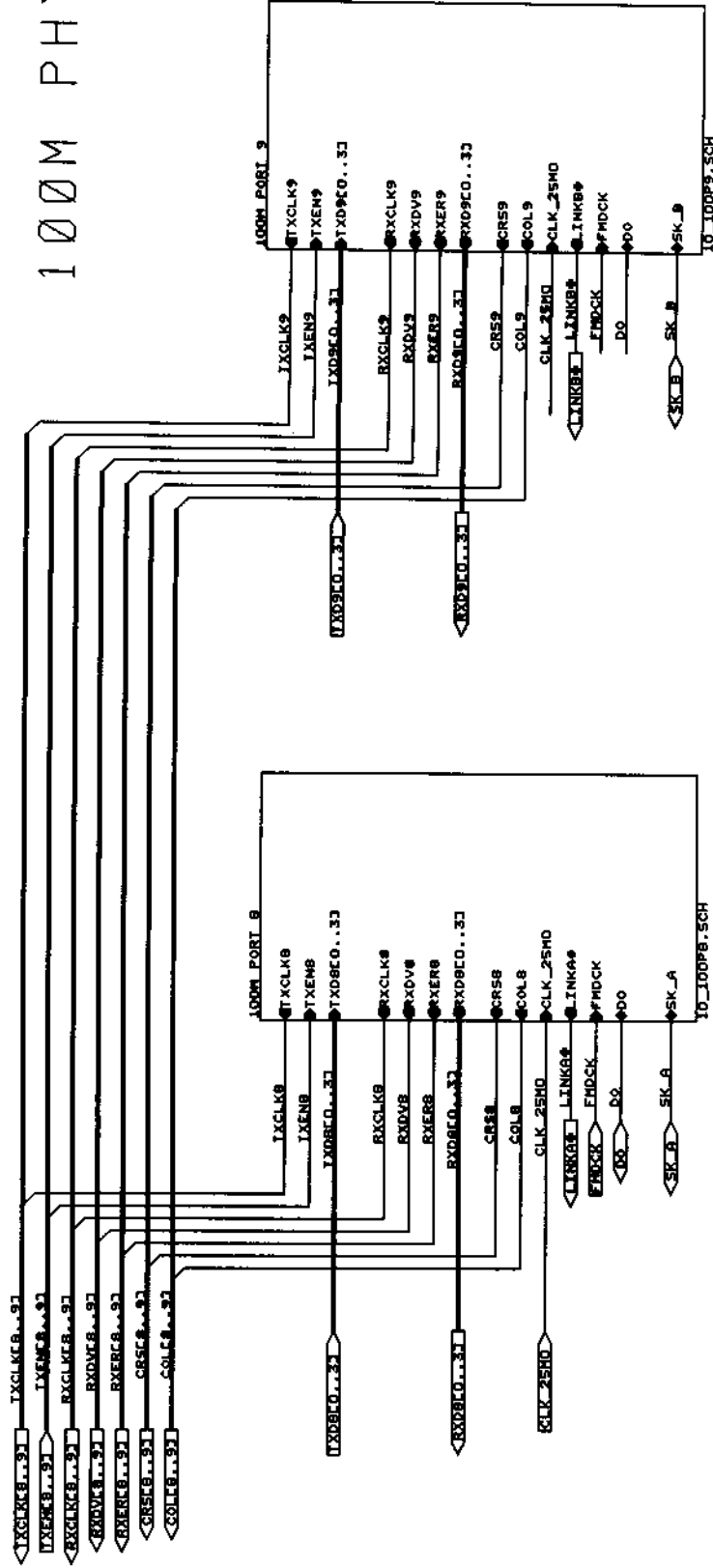


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305DES818---A1-

Prepared :	POLLY MANN
Issued Date :	
By :	
DOS-#	065-810/DOS-810's L.
Disbursement Number:	C
Date:	February 15, 1988

100M PHY



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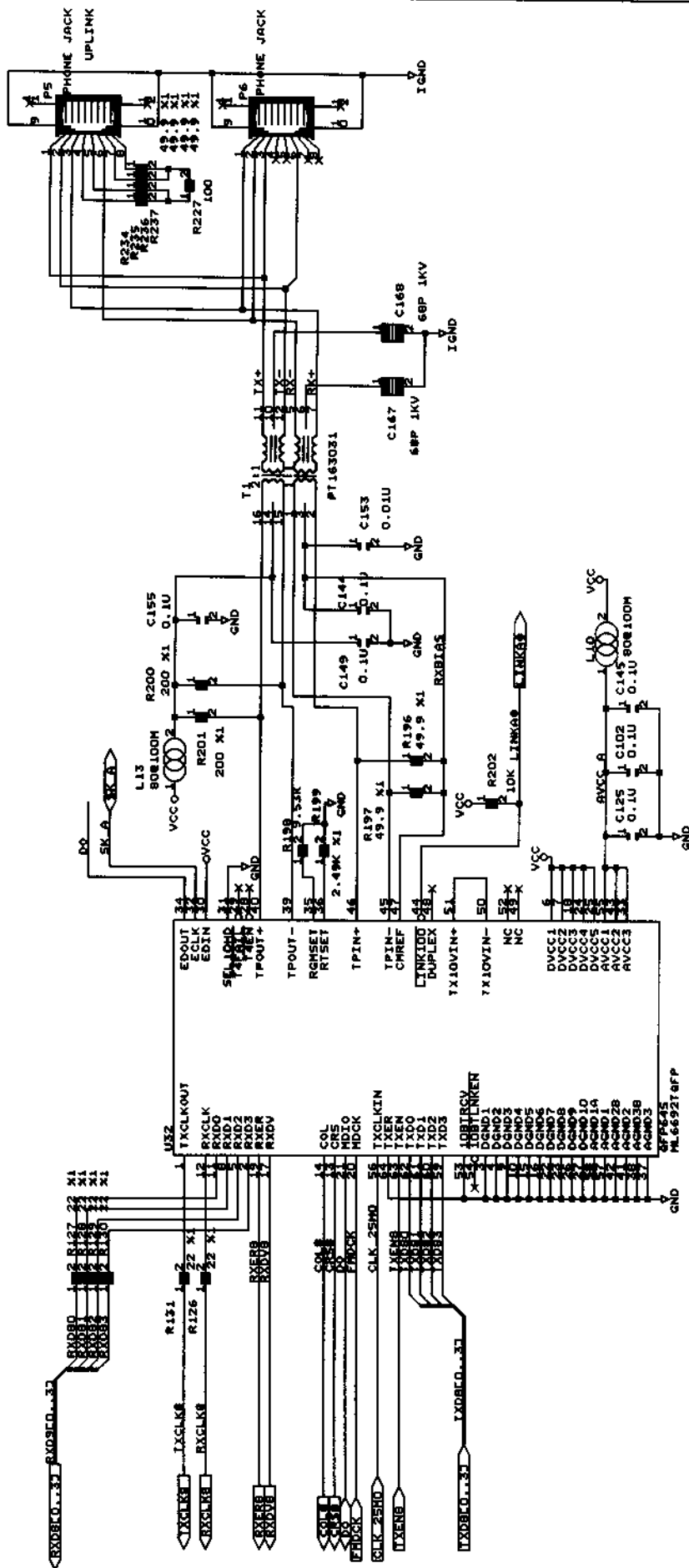
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DOC. NO.: 305DES18---A1-  
Version: A  
Size Document Number: 8  
OEM-0000-00-V10  
Date: March 5, 1997  
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M16592 CAN CONFIG 3 MODES WHEN RESET
A:EDIN C:0000/EDOUT->AS 33C4A5'S DO (CM)
SEL00DUP/CLK->AS 33C4A5'S DO (CM)
SEL00D74/EDOUT->AS 33C4A5'S DO (CM)
B:EDIN High: CUSE LOGIC OR MICRO_P
SEL00DUP/CLK->AS CLK'S INPUT PIN
C:EDIN0000/EDOUT->INPUT 16 DATA AS CLK'S RISING ENGE
M16593 CAN DEFAULT VALUE
PHY ADDRESS=00H
CHANGE SETTING BY MOC/MCIO

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# D-Link

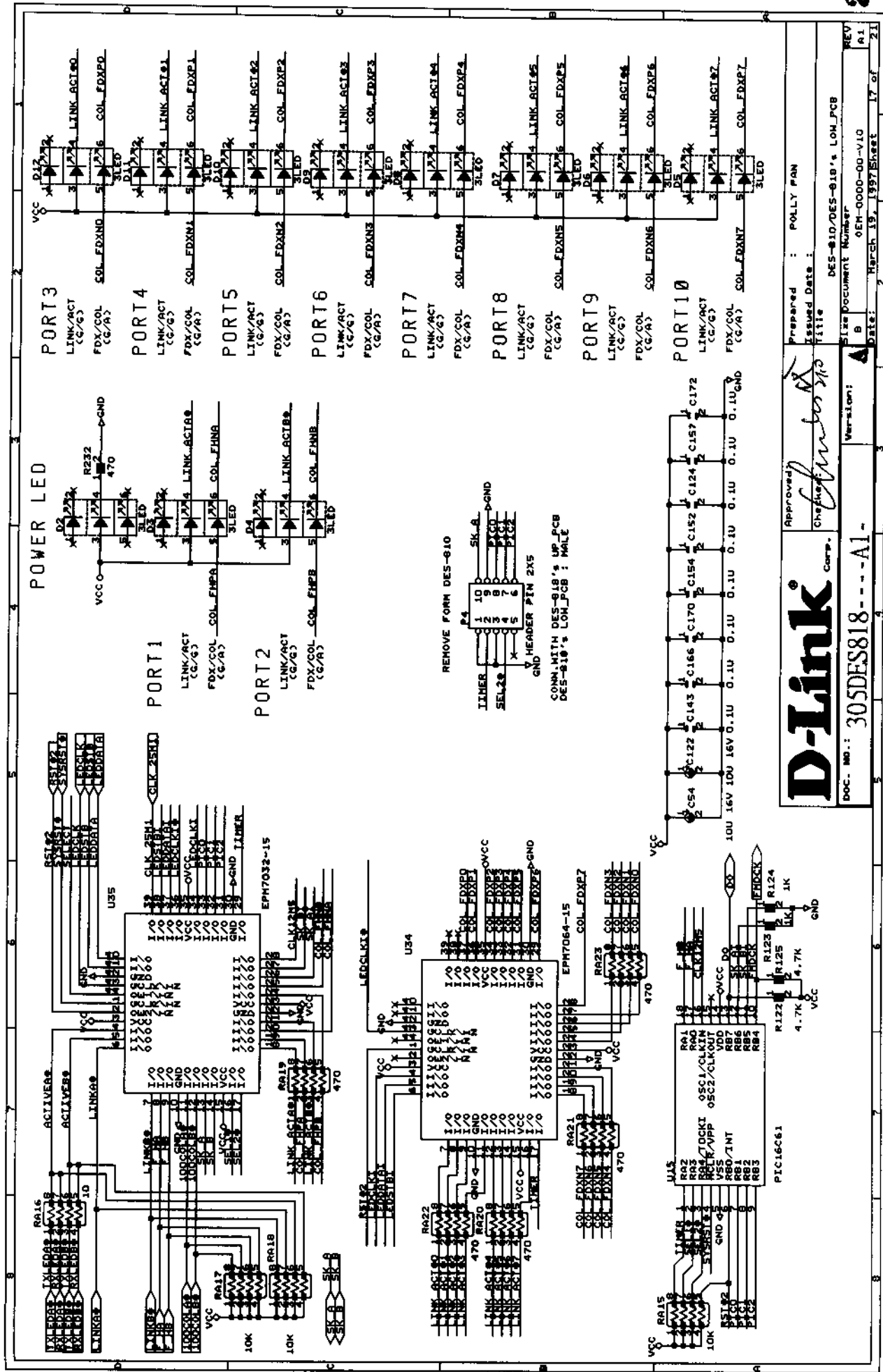
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Version:	Size	Document Number
A	B	
Date:	April 18, 1997	
Sheet	15	

100M PORT2

Approved:	Prepared :	POLLY PAN
Checked: <i>hitesh</i>	Issue Date :	
	Title	

DOC. NO.: 305DES818- --A1-

DES-810/DES-810's LOW_PCB	
Size Document Number	REV
B	A1
Date: April 18, 1997	Sheet 16 of 21



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DOC. NO.: 305DES818---A1-

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 Title : DES-810/DES-819's LON\_PCB  
 Size Document Number : A1  
 Version: 1  
 Date: March 19, 1997 Sheet 17 of 21

Approved: *Chief Engineer*  
 Title: *Chief Engineer*  
 Date: *March 19, 1997*

REMOVE FROM DES-818

VCC

C13  
10uF 16V

BEAD CORE

L2

P2

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20

DES194  
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HEADER PIN 2X20

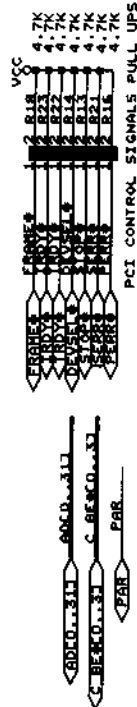
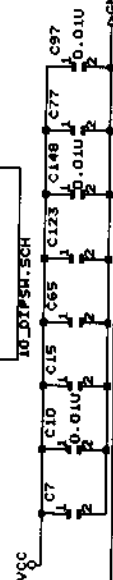
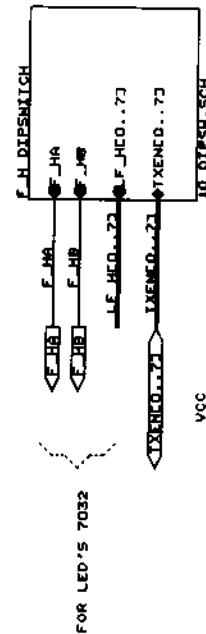
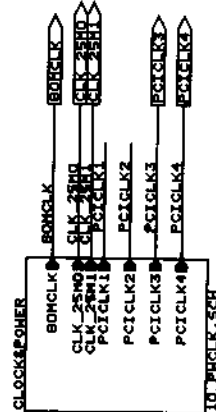
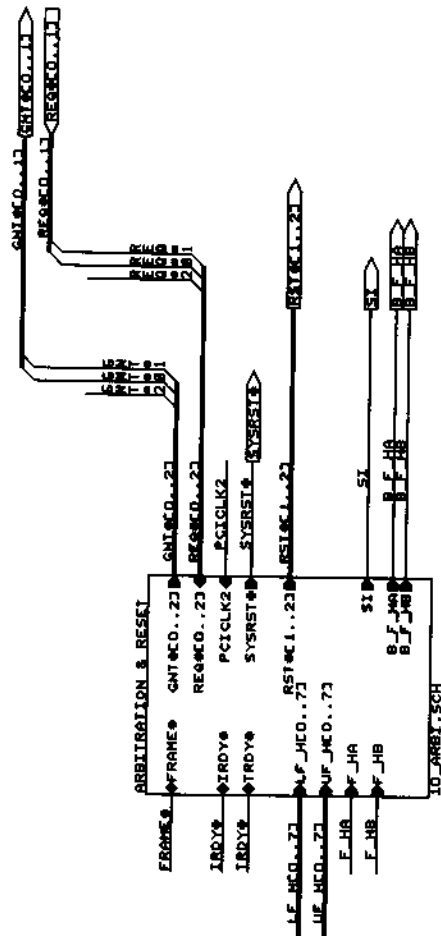
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DES155  
DES154

HEADER PIN 2X20

CONN. WITH DES-818: 1. UP PCB  
DES-818: 2. LOW PCB: 3. MALE



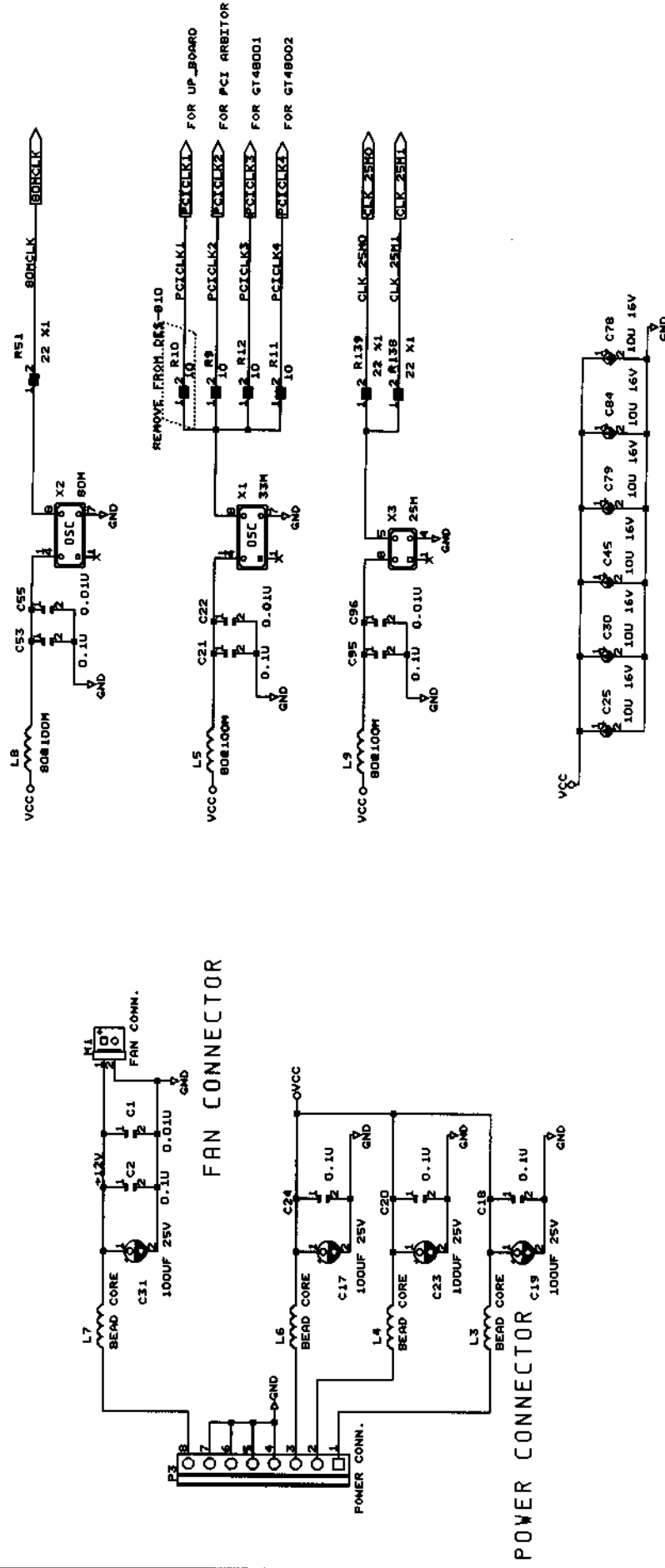
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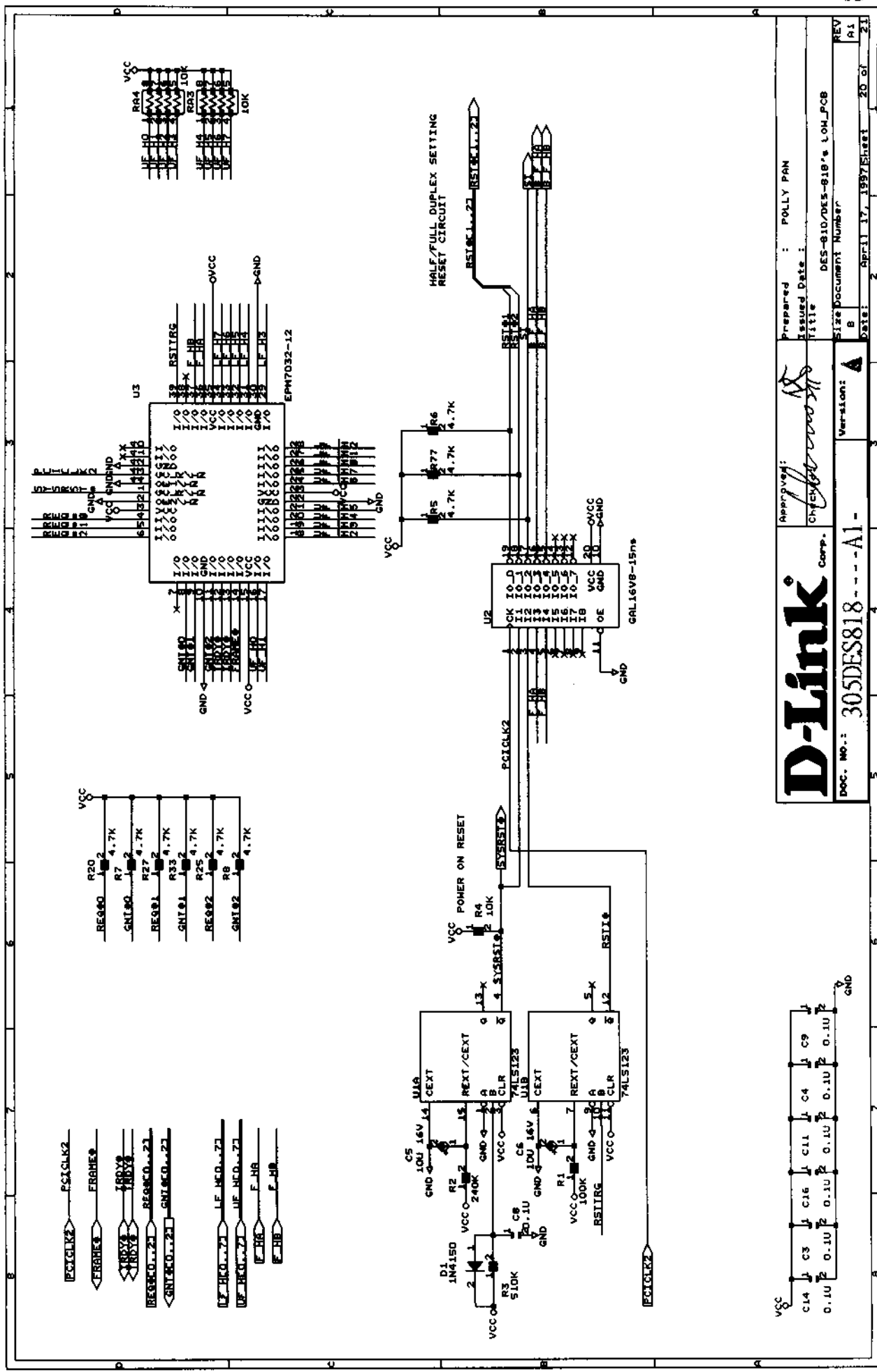
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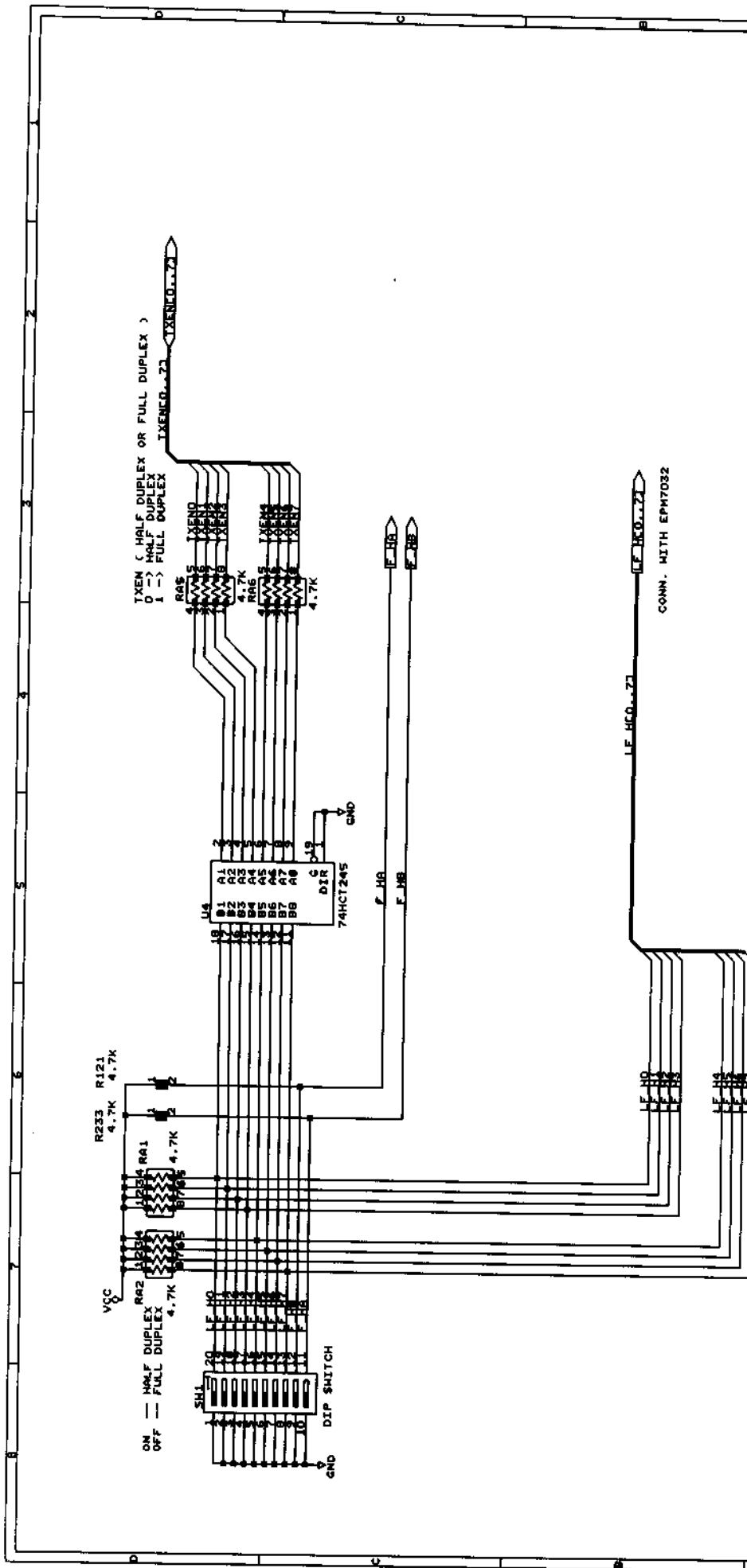


# POWER AND CLOCK GENERATOR



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